Perspectives in Communication, Embedded-Systems and Signal-Processing (PiCES) – An International Journal
ISSN: 2566-932X, Vol. 2, Issue 3, June 2018

Implementation of an Efficient Phase Locked Loop System for 4G Systems

Vishakha
Student, VLSI design and Embedded systems, M.Tech, BNMIT, Bengaluru

Veena S Murthy
Associate Professor, Dept of ECE, BNMIT, Bengaluru

Abstract: With the recent advancements going in the field of engineering, several new models for mobile phones are introduced in the market very often. One of the main judging parameters of these phones is their battery consumption. Thus, a need to develop high speed, low power consuming modules arises. The important module of any communication system is the demodulator circuit. One of the main factors that has to be taken care while demodulating a signal is to detect and correct phase errors, without which meaningless messages can be received. Thus the objective of this project would be to develop a phase locked loop system for error free demodulation.

Keywords: PLL; NCO; Loop filter; Demodulation.

I. INTRODUCTION

Demodulation is the process of extracting the original information message signal from the carrier wave. The important factor is the power consumption in the demodulator circuit and also to get the error free demodulation system. Thus a need to develop high speed and low area modules arise. This can be done by using the costas loop in the demodulator section which gives the error free signals.

A phase locked loop is the system which produces the signal output where the phase is relevant to the input signal phase. PLL is used in the synchronization of the circuit. The costas loop is on the PLL based which is used for the carrier frequency restoration from the suppressed carrier modulated signal and the phase modulation signal like the BPSK and the QPSK signals.

In the costas loop the different architectures for the Numerically Controlled Oscillator and for the FIR filters are implemented. Loop filter block is also designed to check the phase errors. The conventional architecture for NCO is the Look Up Table based where all the values are to be pre calculated and then stored this results in the greater area required and the memory consumption of the NCO increases.

The existing system of FIR filters is based on the Direct form architecture where there is greater need of adders in the circuit which increases the overall area of the system the time required is also more.

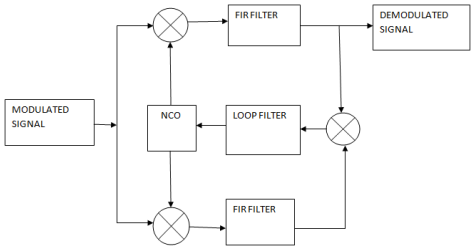

Fig 1. Costas Loop

II. LITERATURE SURVEY

The Zigbee has less data rate, less power usage, reduced cost and shorter length of communication. The synchronization of the carrier by the method of synchronizing symbol and by costas loop by the method of earlier gate timing recovered can be obtained by its receiver but here the execution of the Zigbee transceiver may be improved by synchronizing the frame technique. It may be converted into Hardware Description Language and then dumped into FPGA to obtain the integrated chips [1].

The algorithm is to demodulate the Binary Phase Shift Keying (BPSK) signal of the unidentified frequency and the phase in the extended band radar signal. Here the design was mainly concentrated on getting the phase and the frequency of the carrier wave that may be used to demodulate the BPSK signal. Attribute of the demodulated information rely upon on the Signal to noise ratio (SNR) of the BPSK signal. The SNRs ranging above -70db data can be favorably demodulated. The SNRs under this range give the incorrect or inconsistent answers [2].

A digital application for the revelation and rectification of phase noise applied by fiber network representing the variations in fiber distance is taken exactly with a quick analog to digital converter (ADC) then by a tracking Numerical Controlled Oscillator (NCO). It decreases the components inactivity and interruption in communication among the various parameters rising the bandwidth. The system which is proposed is applied on the Red Pitaya which is an open source stage induced by Zyng, system on chip (SOC) of Xilinx which includes a FPGA and an ARM processor embedded on the single chip [3].

III. IMPLEMENTATION

To generate the message signal we consider the message bits as 1010 or 1200bps and the carrier frequency to be 120 KHz. Hence by multiplying the message and the carrier signal we get the modulated BPSK signal.

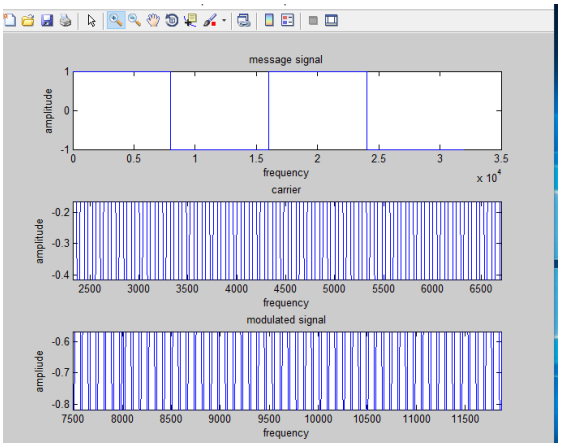

Fig 2. Modulation waveforms

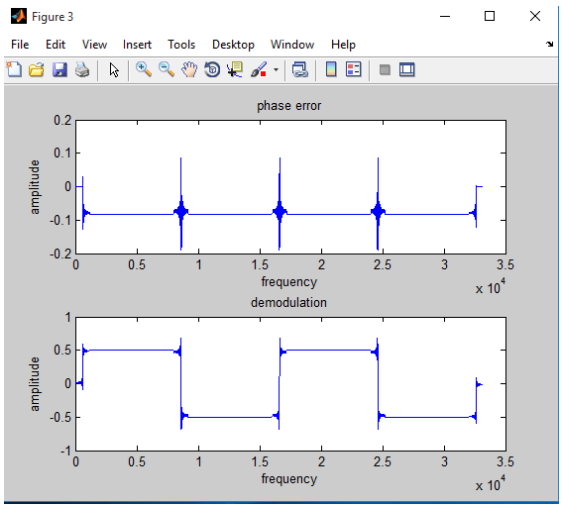

Fig 3. MATLAB Demodulator output

The Verilog implementation of the Numerical Controlled Oscillator architecture mainly consists of the two blocks a phase accumulator and the amplitude generator.

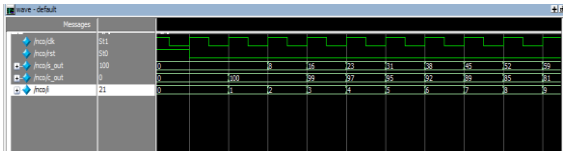

Fig 4. NCO waveforms

The proposed architecture for NCO is based on the Pipelined based architecture it has the cordic system. It has the latency of 12 clock cycles.

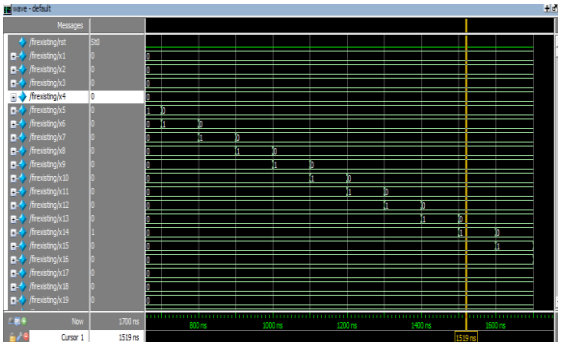

Fig 5. Pipeline architecture waveforms

The existing FIR Filter is based on the Direct form architecture which requires more number of adders in the circuit increasing the system area.

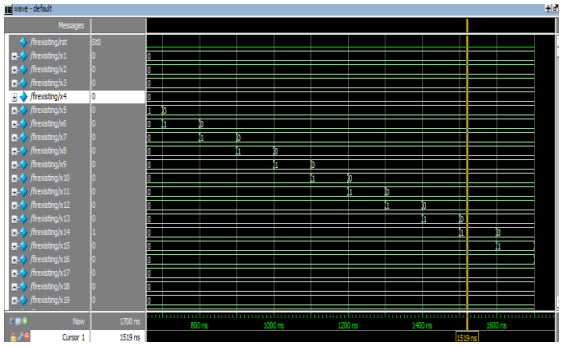

Fig 6. Direct form architecture waveforms

The proposed architecture for the FIR filter is based on the folded architecture where the number of adders required are less when compared to existing form hence helps in reducing the system area.

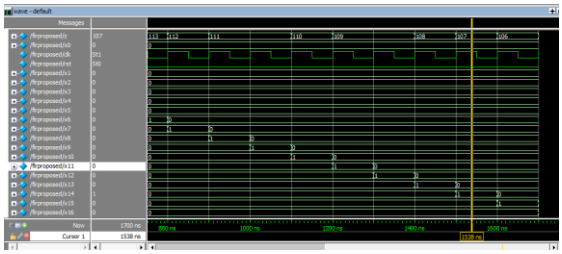

Fig 7. Folded architecture waveforms

Simulink: The block diagram is implemented in the simulink which gives the demodulator output.

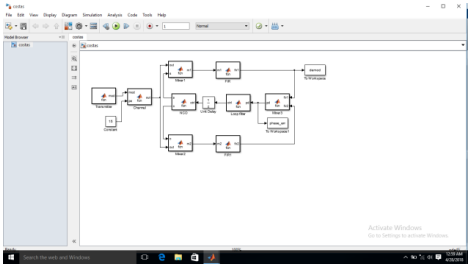

Fig 8. Costas Loop in simulink

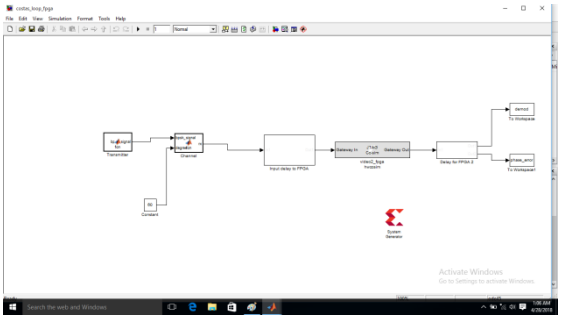

Fig 9. Costas loop in system generator

Xilinx ISE implementation

The Xilinx ISE implementation is done to know the area, power and timing specifications of the NCO, Pipeline, Direct form and the Folded form architectures.

Table 1. Comparison of architectures.

	NCO	**Pipeline**	**FIR existing**	**FIR proposed**
Area Number of slices Number of LUTs (%)	1 1	36 40	42 39	3 19
Timing (ns)	3.7298	8	1.241	1.590
Power (W)	0.066	0.057	3.156	0.368

IV. CONCLUSION

The phase error and power consumption problem in the demodulator circuit can be solved by using the costas loop. The existing FIR filters based on direct form architecture requires more number of adders when compared to the proposed Folded architecture. The power consumption is also less. Hence it gives an efficient PLL based system. The advantage is that the phase error calculation is dynamic. In the future it can be tested for the real time signals like the voice signals.

REFERENCES

[1] Kavya Gorantla and V.V.Mani , "Synchronization in IEEE 802.15.4 Zigbee Transceiver using Matlab Simulink.", International Conference on Advances in Computing, Communications and Informatics (ICACCI), 2015.

[2] Dylon Mutz and Kiran George, "Costas loop and FFT based BPSK Demodulation for Pulsed Radar Receivers", IEEE, 2016.

[3] A. C. Cardenas Olaya, S. Micalizio, M. Ortolano, C. E. Calosso, E. Rubiola and J-M. Friedt, "Digital Electronics Based on Red Pitaya Platform For Coherent Fiber Links", IEEE, 2016.

[4] C.Listad, G. Grosche ,N. Quintin , C. Shi et al. "A clock network for geodesy and fundamental science",arXiv:1511.07735.

[5] C.E. Calosso,E. bertacco, D. Calonica, C. Clivati, G.A. Costanzo, M. Frittelli, F. Levi, S. Micalizio, A.Mura, A. Godone, "Doppler-stabilized fiber link with 6 dB noise improvement below the classical limit", Lett. 40, No. 2, 131 (2015).

[6] M. Yuldashev, Mathematical models and simulation of Costas Loops,University of Jyvaskyla,2013.

[7] G.Gupta(2011,September). Costas Loop [online]. Available: http;//www.mathworks.com

[8] P.Shachi, R.Mishra and P.K.Jatoh."Coherent BPSK demodulator using Costas Loop and early gate synchronizer", IEEE,2013,pp. 975-980.