Perspectives in Communication, Embedded-Systems and Signal-Processing (PiCES) – An International Journal
ISSN: 2566-932X, Vol. 1, Issue 5, August 2017
Proceedings of National Conference on Emerging Trends in VLSI, Embedded and Networking (NC-EVEN 17), May 2017

Design and Stability Analysis of CNTFET Based SRAM Cell

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Abstract: Electronic gadgets like computers usually rely on memory devices because the digital information must be stored in these memory devices. Among many memory devices available Static Random Access Memory (SRAM) is the most crucial one. Due to continuous scaling of CMOS technology, it limits the performance of 6T SRAM cell in terms of leakage power. So carbon nanotube field effect transistor (CNTFET) are widely studied as possible alternative. Verilog-A code of CNTFET based SRAM cell is simulated in Cadence Virtuoso Tool. Here the conventional 6T SRAM cell is compared with CNFET based SRAM cell.

Keywords: CNTFET; SRAM

I. INTRODUCTION

SRAM is nothing but an array of flip flops. SRAM does not need to be refreshed. SRAM is cheaper when compared to DRAM because DRAM is usually 1.5 to 4 times dense than SRAM. In order to keep up Moore's law, the transistor size has to be decreased. But as the scaling increases, the stability of the transistor was major concern. Carbon nano tubes are widely studied as an alternative for silicon based transistor. Most important memory is the cache memory. But in microprocessors cache occupies more than 50% of chip area. The main reason for power dissipation is the leakage power of cache.

To reduce power dissipation supply voltage should be scaled down, which exponentially increases the subthreshold leakage current and thus leads to increment in the leakage power.

SRAM cell operates in 3 modes: Read operation, Write operation and Standby operation. In read operation the bit lines are pre-charged to high level (Vdd). The word line is also high so the access transistors are on and the information is sensed on bit lines. For write operation word line is high and the access transistors are turned on and the data is imposed on the bit lines. For standby operation, the word line is low. So the access transistor are off hence the inverters are in complementary state. The conventional 6T SRAM cell is shown in Fig. 1.

Carbon nano tubes are hexagonal sheets of graphene which are rolled up into hollow cylinder. A carbon nano tube's bandgap is directly affected by its chirality and diameter. In traditional MOSFET structure channel material is made up of bulk silicon, this can be altered by using single carbon nano tube or an array of carbon nano tubes. This kind of Field EffectTransistor is called Carbon Nano Tube Field Effect Transistor (CNTFET).

Like CMOS, CNTFET's also has complementary devices like cnfet and cpfet. The p-type transistors conducts holes and n-type conducts electrons. CNTFET works on the principle of direct tunnelling through a Schottky barrier at the source channel junction. The gate voltage can control the electrical conductance of CNTFET by changing electron density in the channel [1].

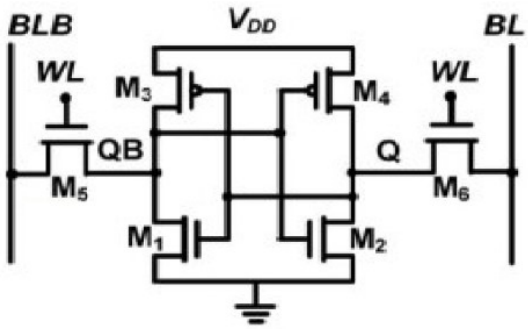

Fig 1. Conventional 6T SRAM cell

II. LITERATURE SURVEY

In a paper to evaluate the potential of carbon nanotube field effect transistors (CNFETs) to replace silicon CMOS technology, they developed a SPICE model of CNFET nanoelectronics. Their model is parameterizable, and it enables composition of models of various aspects of nanoelectronic behaviour [2].

A new DC thermal model of Carbon Nanotube Field Effect Transistors (CNTFETs) was proposed. The model is based on a number of fitting parameters depending on bias conditions by third order polynomials. The model includes three thermal parameters describing CNTFET behaviour in terms of saturation drain current, threshold

voltage and M exponent in the knee region versus the temperature [3].

The steady reduction in the dimension of transistors, according to Moore's law has been the main force behind the regular leaps in the level of performance of the silicon ICs. Due to the effects like the short channel effects, tunneling effect, additional heat dissipation, interconnect problems etc problems arise. So it is not possible to reduce the size further. Hence now it is necessary to adopt new material or technology. Carbon Nano Tube Field Effect Transistors (CNTFETs) are being widely studied as possible successors to silicon MOSFETs. This paper focuses on simulation of CNTFET based digital circuits using HSPICE [4].

CMOS RAM Cell is very less power consuming and has very less read and writes time. As the technology is improving channel length of MOSFET is scaling down. In this environment stability of SRAM becomes the major concern for future technology. A SRAM cell must meet requirements for operation in submicron/nano ranges. So we have to modify conventional 6T SRAM circuit with additional circuitry and different kind of parametric analysis can be done and functionality is verified using Cadence Design Environment for 90nm technology files [5].

III. PROPOSED WORK

The fundamental part of SRAM cell is an inverter. The p-type CNTFET is the pull up network (PUN) and the n-type CNTFET is the pull down network (PDN). The pull up network is connected to high supply Vdd and the pull down network is connected to ground. The CNTFET based inverter circuit is shown in fig. 2.

SRAM cell is constructed using two inverters each having one n-type CNTFET and one p-type CNTFET. The drain terminals of these transistors are connected to storage nodes Q and QB. The gates of these transistors are crossed couples. Two access transistors (A1, A2) are n-type CNTFET's, which are controlled by word-line WL through gate. These access transistors connect the bit lines (BL, BLB) to the inverter outputs. A value 0 or 1 is loaded (write) or accessed (read) from the cell through bit-lines (BL, BLB). CNTFET based SRAM cell is shown in fig. 3. In the nano tube device, the transistor action occurs at the contact points between the metal electrodes and the carbon nano tube.

IV. SIMULATION AND RESULT

The code for n-type CNTFET and p-type CNTFET is written in Verilog-A format. This code is stored as symbol or block in a separate library of cadence. This symbol is used to draw theschematic diagram. When word-line is high, Q and QB changes according to BL and BLB. When word-line is low, Q and QB retain their states.

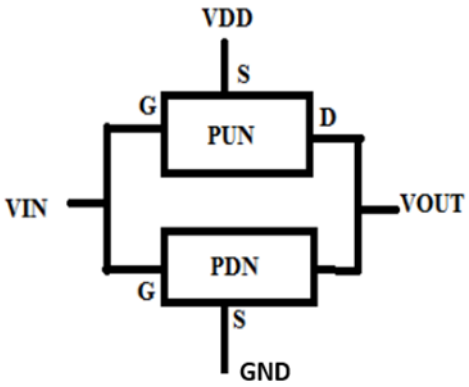

Fig 2. CNTFET based inverter

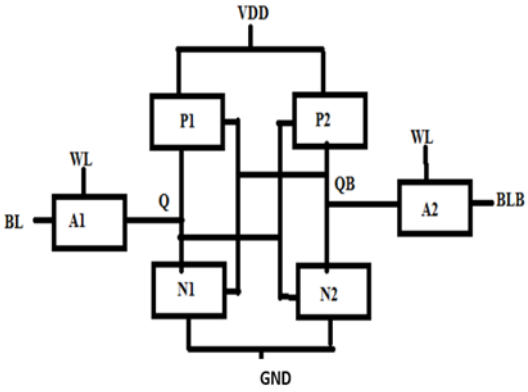

Fig 3. CNTFET based inverter

The inverter schematic diagram is shown in fig. 4. The output of the inverter is shown in fig. 5. Using two inverters SRAM cell is designed and is as shown in fig. 6. The final output waveforms of CNTFET based SRAM cell is shown in fig. 7.

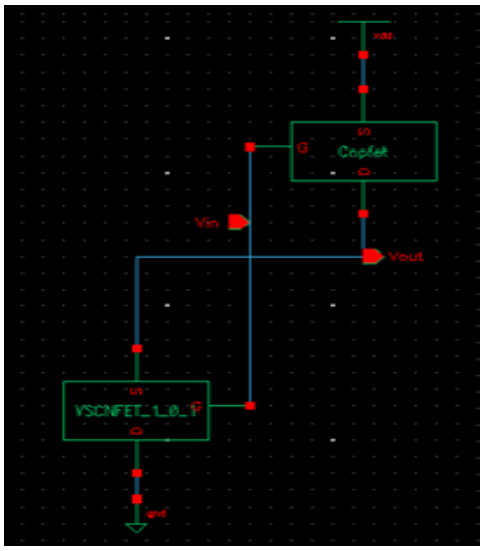

Fig 4. Schematic of inverter

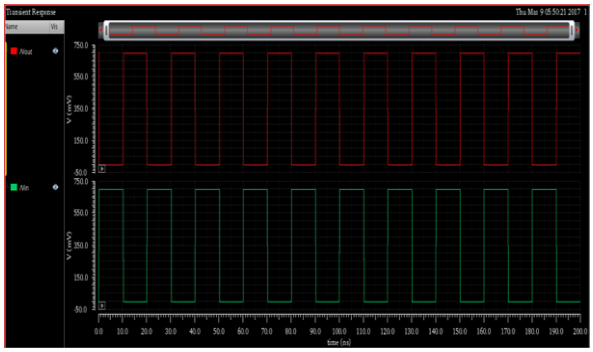

Fig 5. Output waveform of inverter

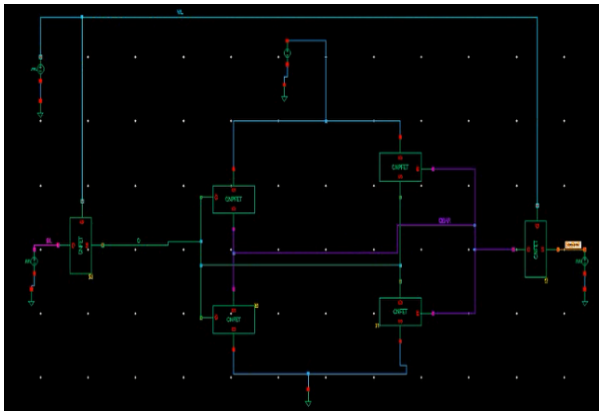

Fig 6. Schematic of CNTFET based SRAM cell

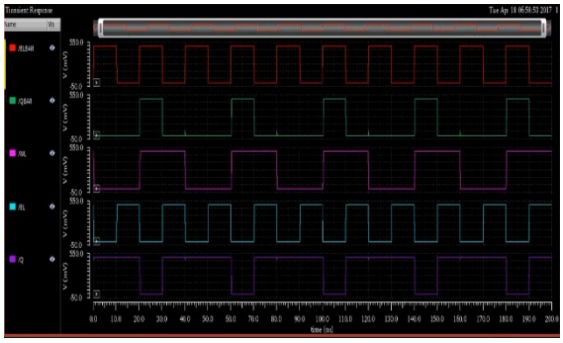

Fig 7. Output waveforms of CNTFET based SRAM cell

Performance parameters	Conventional 6T SRAM cell in 45nm	CNTFET based SRAM cell
Leakage power (W)	989 mW	377 mW
Delay (sec)	29.93 ns	217 ps

Table 1. Performance

V. CONCLUSION

In this paper we have proposed the CNTFET-based SRAMcell. It is compared with the CMOS-based 6T SRAM cell in 45nm technology. An improved result was exhibited by CNTFET based.

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