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Three-Phase Inverter with Energy Buffer and DC-DC Conversion Circuits

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Abstract: This paper proposes a new Three-phase inverter topology and describes the control method for the proposed inverter. The inverter consists of an energy buffer circuit, a dc-dc conversion circuit and an H-bridge circuit. The energy buffer circuit and H-bridge circuit enable the proposed inverter to output a multilevel voltage according to the proposed pulse width modulation (PWM) technique. The dc-dc conversion circuit can charge the buffer capacitor continuously because the dc-dc conversion control cooperates with the PWM. Simulation results confirm that the proposed inverter can reduce the voltage harmonics in the output and the dc-dc conversion current in comparison to a conventional inverter consisting of a dc-dc conversion circuit and H-bridge circuit. Experiments demonstrate that the proposed inverter can output currents of low total harmonic distortion and have higher efficiency than the conventional inverter. In addition, it is confirmed that these features of the proposed inverter contribute to the suppression of the circuit volume in spite of the increase in the number of devices in the circuit.

Keywords: Energy buffer circuit; single-phase inverter; dc-dc conversion; pulse width modulation.

I. INTRODUCTION

Single-phase inverters are commonly used in many power applications. In recent years, single-phase inverters have been used as components of microgrid systems. In these systems, single-phase inverters are used as interfaces for renewable energy sources, such as fuel cells and photovoltaic energy, or for energy storage devices, such as batteries and ultracapacitors with the grid [1]–[7]. Various types of single-phase transformerless inverters, which have the advantages of a small size and a light weight [8], have been studied [9]–[12]. Among these, H-bridge inverters have a relatively simple structure. The H-bridge inverters, however, suffer from common-mode voltage unlike inverters such as H5 inverter, HERIC inverter and H6 inverters. In applications using batteries and ultracapacitors with output ratings of less than several hundreds of watts, the H-bridge inverter may be able to perform without the influence of the common-mode voltage. On the other hand, in applications with photovoltaic cells, the common-mode voltage causes a leakage current through parasitic capacitors between the photovoltaic cells and the ground. The leakage current degrades the performance and reliability of the inverter. However, this disadvantage can be mitigated with passive filters [13]–[15] and therefore the H-bridge inverter can be used in wide applications.

An inverter consisting of an H-bridge circuit involving a dc-dc conversion circuit can expand the voltage amplitude of the output. Therefore, this type of inverter is commonly used in applications for renewable energy sources and energy storage devices with voltages that are lower than the voltage amplitudes of the grid. The typical topologies for the dc-dc conversion are boost, and buck boost converters in addition to many other types of converters derived from these chopper topologies, including chopper inductors [16]–[18].

Inverters with an energy buffer circuit have been previously reported in [19]–[22]. An energy buffer circuit consists of switches and buffer capacitors and behaves like a charge pump circuit. Because the energy buffer circuit does not include any inductors, it can be designed with a compact form. The operation of the circuit allows the inverter to step up its dc link voltage with the help of the voltage across the buffer capacitors. Furthermore, it allows the inverter to yield a multilevel output voltage. It is well known that in multilevel inverters, the output voltage can reduce ripple in the output current, resulting in a lower output filter inductance [23]–[32]. Although the multilevel inverters have more output voltage vectors than the inverter with an energy buffer circuit, they generally cannot expand the voltage amplitude of the output.

However, inverters with only an energy buffer circuit have difficulty regulating the voltage of the buffer capacitor because the capacitor can be charged only when the inverter outputs a low voltage [20], [21]. Therefore, inverters containing both an energy buffer circuit and a dc-dc conversion circuit have been proposed [33], [34]. The variation in the energy of the buffer capacitor can be compensated for by the dc-dc conversion circuit. The multilevel energy buffer (MEB) inverter, which consists of the same circuit combination, has been proposed as part of the MEB micro-inverter in [33] and has been reported to have high efficiency and to allow a small filter inductance.

This paper proposes a new single-phase inverter topology with an energy buffer circuit, a dc-dc conversion circuit, and an H-bridge circuit. It has different configuration from the MEB inverter in [33], in particular, in terms of connection of the dc-dc conversion circuit. The most important thing is that the difference brings the following strong advantages over the MEB inverter to the proposed inverter: Although the dc-dc conversion circuit in the MEB inverter cannot charge or discharge the buffer capacitor during the step-up operation because of the circuit configuration, the dc-dc conversion circuit in the proposed inverter can continuously charge of discharge it regardless of operation mode. For this reason, the voltage variation of the buffer capacitor of the proposed inverter can be suppressed (refer to Appendix A) or the capacitance of the proposed inverter can be a smaller value. Furthermore, in general, the continuous charge operation is more effective than the intermittent charge operation; therefore the proposed inverter can be operated with more effective performance than the MEB inverter.

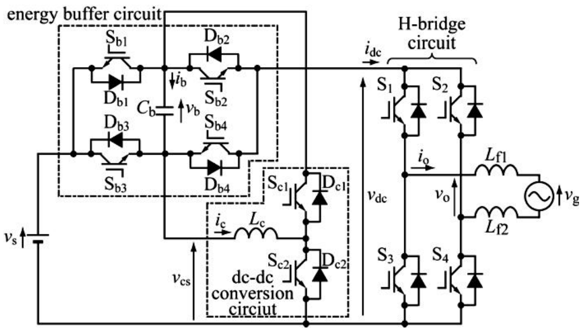

Fig 1. Configuration of proposed single-Phase inverter

	V_{dc}	Switching signals
Mode1	$vs–vb$	ON:Sb1 and Sb4 OFF :Sb2 and Sb3
Mode2	vs	ON:Sb3 and Sb4 OFF :Sb1 and Sb2 or ON:Sb1 and Sb2 OFF :Sb3 and Sb4
Mode3	$vs+vb$	ON:Sb2 and Sb3OFF :Sb1 and Sb4

Table 1. Modes of operation of Energy Buffer Circuit

For the proposed inverter, a pulse width modulation (PWM) technique for dc-ac and ac-dc conversions and a control technique for the dc-dc conversion circuit are described in this paper. The energy buffer circuit and H-bridge circuit are operated according to the PWM technique and yield multilevel outputs following the voltage command signal. Control of the dc-dc conversion circuit enables the circuit to charge the buffer capacitor continuously by cooperating with the PWM Simulation results confirm that the proposed inverter can reduce the voltage harmonics in the output and the dc-dc conversion current in comparison to a conventional inverter consisting of a dc-dc conversion circuit and H-bridge circuit. Experiments demonstrate that the proposed inverter outputs a current with low total harmonic distortion (THD) and have higher efficiency than the conventional inverter. Furthermore, it is confirmed that these features contribute to the suppression of the circuit volume in spite of an increase in the number of devices.

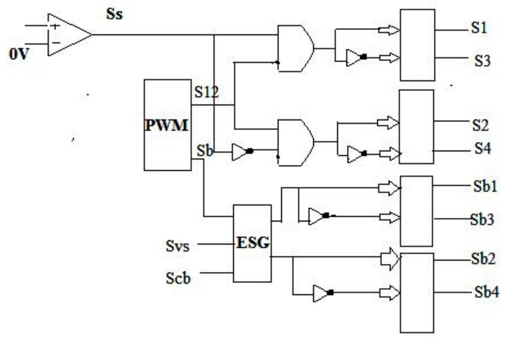

Fig 2. Block diagrams of output voltage control for dc-ac conversions.

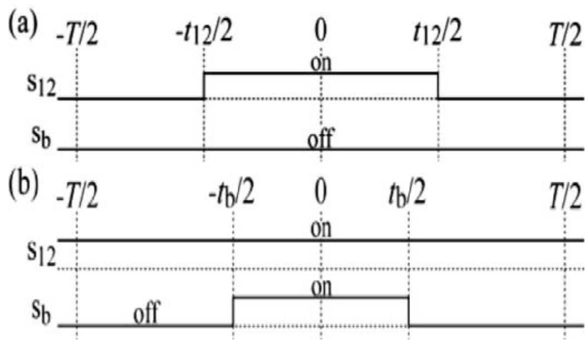

Fig 3. Signal sequences during PWM period when |voc |is in (a) Range I and (b) Range II or III.

II. Circuit Configuration And Control Method

A. Circuit configuration

Fig. 1 shows the configuration of the proposed inverter, which consists of an energy buffer circuit, a dc-dc conversion circuit, and an H-bridge circuit. The inverter is connected to the grid vg through filter inductors L_{f1} and L_{f2}. The energy buffer circuit has four switches, four diodes, and a buffer capacitor C_b. The capacitor C_b has a positive voltage vb. The energy buffer circuit positively or negatively superimposes v_b on the supply voltage v_s and sets the dc link voltage v_{dc} to one of three levels depending on the state of the signals of switches S_{b1} S_{b4}, as given by Table I. When the energy buffer circuit operates in Mode 1, it steps down the dc link voltage v_{dc} to $v_s–v_b$. In Mode 2, the dc link voltage v_{dc} is equal to v_s. The stepped-up voltage v_s+v_b is provided when the energy buffer circuit operates in Mode 3. Although, in Modes 1 and 3, the energy in the buffer capacitor is changed by the dc link current i_{dc}, the dc-dc

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conversion circuit consisting of two switches, two diodes, and the chopper inductor L_c is operated to maintain v_b at a constant level. The H-bridge circuit performs dc-ac or ac-dc conversion, cooperating with the energy buffer circuit.

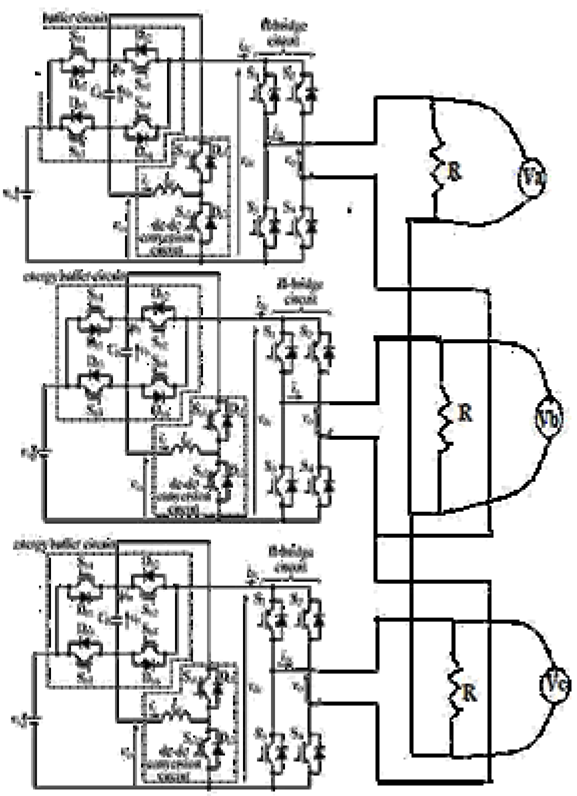

Fig 4. Configuration of proposed Three-Phase inverter.

B. Control for Closed loop operation

The signals are generated based on these durations, as shown in Fig. 3. Based on the energy buffer circuit signal generator (ESG), being a logic circuit, selects the appropriate mode for the energy buffer circuit, regardless of s_{cb}, and assigns corresponding states to s_{b13} and s_{b24}, as given by Table II. When s_b is in the on-state, the energy buffer circuit operates in Mode 2, regardless of s_{vs}. As shown in Table I, operation in Mode 2 can be implemented under two sets of signal conditions, which are determined, based on the state of s_{cb} as follows: When s_{cb} is in the on-state, s_{b13} and s_{b24} are also in the on-state; otherwise, s_{b13} and s_{b24} are in the off-state.

Using this control technique, the energy buffer circuit can generate the dc link voltage waveform conceptually shown in Fig. 5(a). While $|v_{oc}|$ is in Range II or III, the dc link voltage v_{dc} has a PWM waveform with levels of v_s - v_b, v_s, and v_s+v_b. Conversely, while $|v_{oc}|$ is in Range I, v_{dc} is maintained at v_s - v_b. The variation of the dc level is converted to a voltage variation of the ac level by the H-bridge circuit and is formed into an approximately sinusoidal wave following as shown in Fig. 5(b). The H-bridge circuit is operated based on s_s and s_{12}. The signal s_s, which express the sign of v_{oc}, is referenced to assign a polarity to the voltage with the dc level. The signal s_{12} is employed to convert the voltage of v_s-v_b to a portion of an approximately sinusoidal wave with three levels, i.e v_s-v_b, - v_s+v_b, and zero.

Input			Output		Mode of energy
sb	*svs*	*scb*	*sb1*	*sb24*	*buffer circuit*
0	0	0	1	0	Mode1
0	0	1	1	0	
0	1	0	0	1	Mode3
0	1	1	0	1	
1	0	0	0	0	Mode2
1	0	1	1	1	
1	1	0	0	0	
1	1	1	1	1	

Table 2. Truth Table For ESG

The MEB inverter in [33] employs a different PWM technique from this technique. The PWM technique of the MEB inverter uses the zero voltage as one of the voltage pulses, regardless of the range of $|v_{oc}|$; therefore, the voltage harmonics in the output of the MEB inverter are larger than those of the proposed inverter.

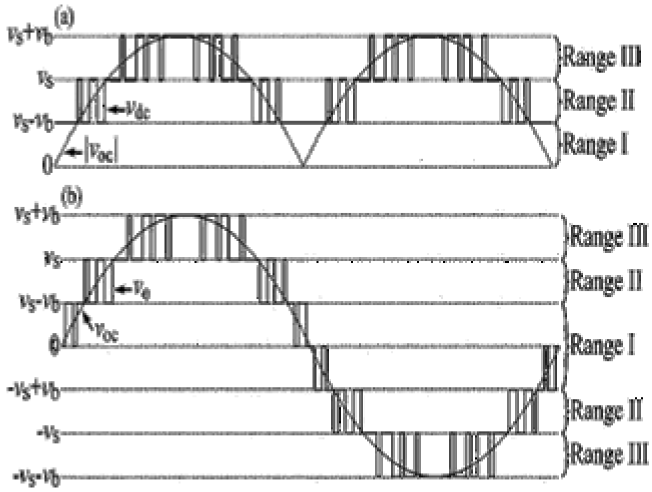

Fig 5. Conceptual waveforms for (a) dc link voltage v_{dc} and (b) Output voltage

C. Control for dc-dc conversion circuit

The operation of the energy buffer circuit in Modes 1 and 3 changes the capacitor voltage v_b, which is controlled at a constant level by the dc-dc conversion circuit. Fig. 6 shows the modes of operation for the conversion circuit. The states of signals s_{c1} and s_{c2} for switches s_{c1} and s_{c2} in the circuit are complementary to each other. When s_{c1} is in the on-state, current through L_c, the path of which is depicted in Fig. 6(a), charges or discharges C_b. When s_{c2} is in the on-state, there are two possible current paths, depending on the states of s_{b1} and s_{b3} for the energy buffer circuit. When s_{b1} is in the on-state the current flows as shown in Fig. 6(b). As a result of switching s_{c1} and s_{c2}, the conversion circuit behaves either like a buck converter when C_b is charged or like a boost converter when C_b is discharged. Alternatively, when s_{b3} is in the on-state, the current path is illustrated in Fig. 6(c) and the conversion circuit acts like a buck-boost converter. The former behavior of the conversion circuit can more effectively regulate V_b because the current continues flowing through V_b during a complete PWM period.

Fig. 7 shows the control block diagram for the dc-dc conversion circuit. The current command signal i_{cc} is calculated to maintain V_b at the command value V_{bc}; then the current i_c through the inductor L_c is controlled by each PI control block to follow i_{cc}. The resulting voltage command signal V_{cc} is used to generate the signals s_{c1} and s_{c2} in the PWM block.

Fig. 8 shows the sequences for s_{c1} and s_{c2} during a PWM period.

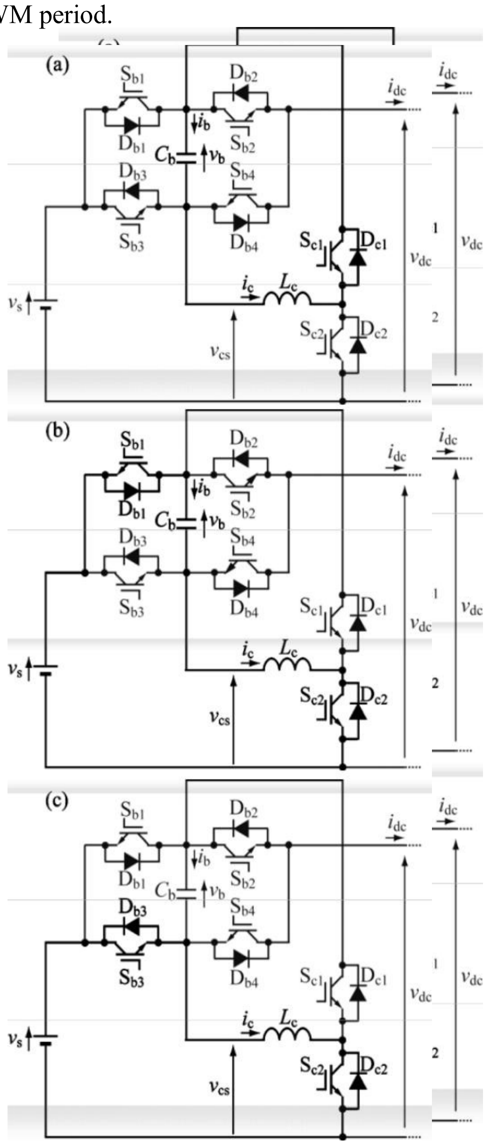

Fig 6. Modes of operation of dc-dc conversion circuit: (a) on-state of s_{c1}, (b) on-states of s_{c2} and s_{b1}, and (c) on-states of s_{c2} and s_{b3}.

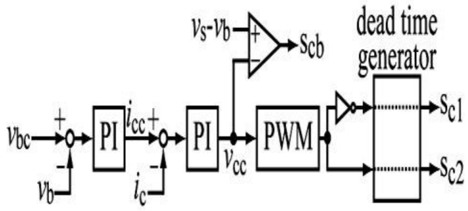

Fig 7. Control block diagram for dc-dc conversion circuit

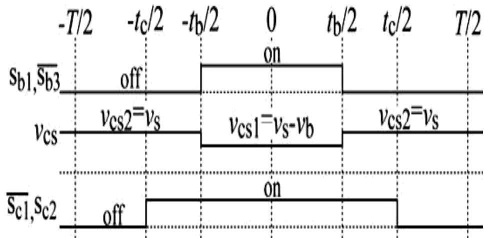

Fig 8. Signal sequences for dc-dc conversion circuit during PWM period.

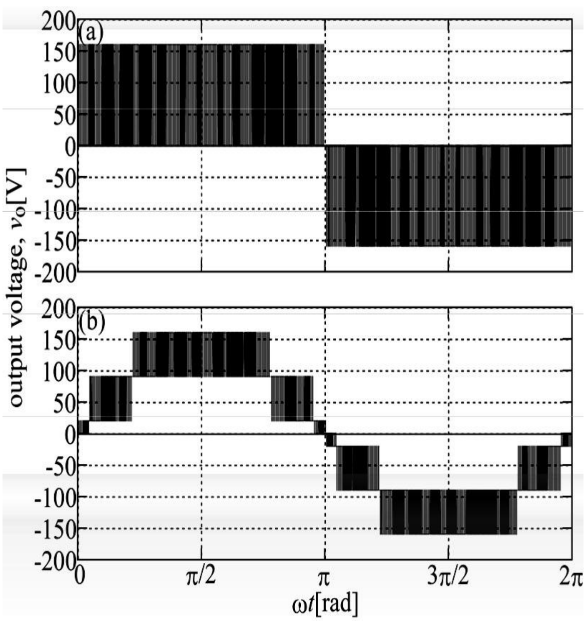

Fig 9. Simulated waveforms of output voltages of (a) conventional inverter with V_s = 160 V and (b) proposed inverter with V_s= 90 V and V_b = 70 V. Effective value V_{oc} of output voltage command signal is set at 100 V.

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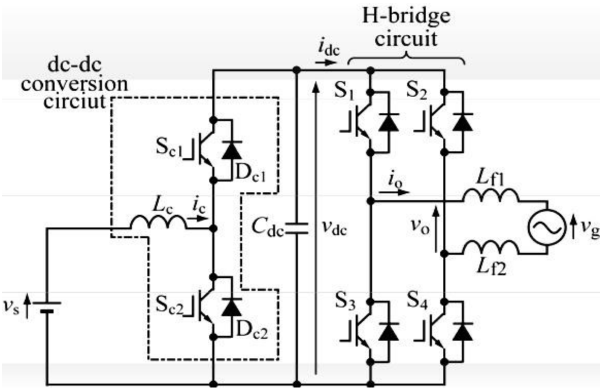

Fig 10. Conventional inverter with dc-dc conversion circuit

III. SIMULATIONS

A. Output voltage and its harmonics

Fig. 9 compares the simulated waveforms of the output voltages on the conventional inverter shown in Fig. 10 with those for the proposed inverter. The results confirm that the proposed inverter produces a multilevel output voltage. Fig. 11 shows the harmonics in the output voltage. The maximum values of the harmonic voltage appear at 40 kHz, which corresponds with a PWM frequency. The conventional inverter has a maximum voltage of 48 V, which is 2.2 times higher than the maximum of harmonic voltage produced by the proposed inverter under the conditions Vs = 90 V and Vb = 70 V. Therefore, the proposed inverter can reduce the inductance of the filter inductors Lf1 and Lf2 at the same PWM frequency.

B. Charged energy and conversion current

Fig.12 shows the power Pb inputted into the buffer capacitor Cb during the operation of the energy buffer circuit and the resulting energy Ub stored in Cb during one cycle of the grid in the dc-ac conversion. The power Pb and energy Ub vary depending on the command voltage voc as follows. Pb is a positive value and Ub increases when |voc| is in Ranges I and II; then Ub peaks at α2, where |voc| is equal to Vs. In contrast, Pb is a negative value and Ub decreases in Range III; Ub reaches a valley at π- α2. In the ac-dc conversion, the power Pb and the energy Ub vary in the opposite manner: for example, Ub increases in Range III and, otherwise, decreases.

Fig. 12 shows the dependence of the energy variation ΔUb on the dc supply voltage vs during the dc– ac conversion. The capacitor voltage Vb is set to 160- Vs. It is found that the variation becomes zero only at Vs = 117V. Therefore, when the voltage vs is not 117 V, to compensate for energy variation and then maintain Vb at a constant value, the dc-dc conversion circuit must be operated.

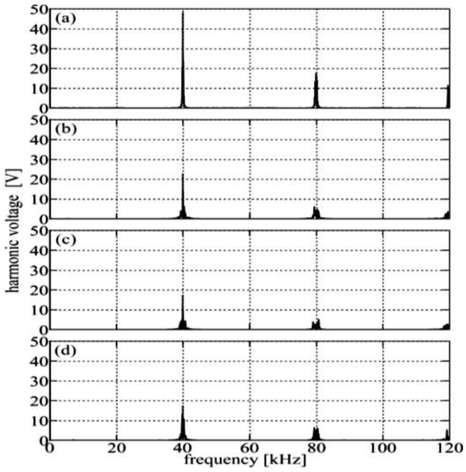

Fig 11. Harmonics in output voltages of (a) conventional inverter with v_{dc} = 160 V and proposed inverter with (b) v_s= 90 V and v_b = 70 V, (c) v_s = 110 V and v_b = 50 V and (d) v_s = 130 V and v_b = 30 V, under v_{oc} = 100 V.

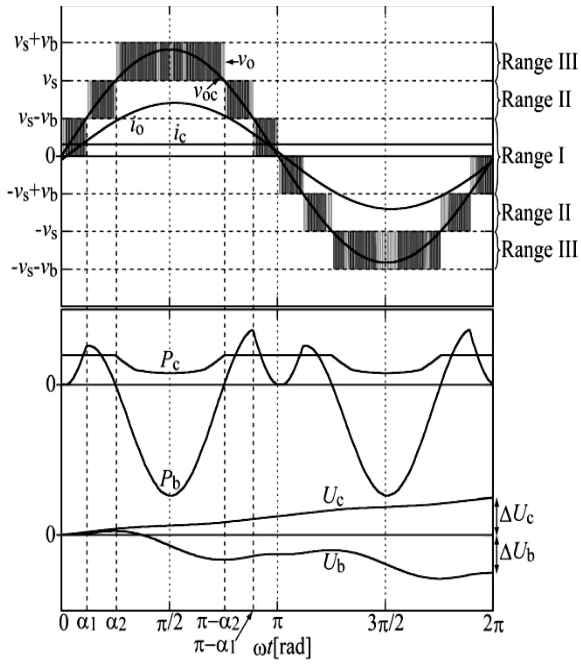

Fig 12. Input powers and stored energies of C_b during one cycle

The dc-dc conversion current i_c is controlled at a constant value during one cycle of the grid. The power Pc transferred into C_b from the dc-dc conversion circuit varies as shown in Fig. 11. The power varies depending on the state of the signals Sb1 and Sb2. The power remains at a low level while |voc| is in Range III because sb3 is often in the on-state in this range. On the other hand, the power reaches a high level in Ranges I and II because sb1 is always in the on-state. It is noted that, in Fig. 11, the signal sb1 is assumed to be in the on-state when the energy buffer circuit is operated in Mode 2. In

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contrast, if sb3 is in the on-state in Mode 2, the power P_c would move toward a lower level in Ranges II and III. The energy U_c is an integration result of Pc and represents the energy transferred into C_b from the dc-dc conversion circuit. When the energy variation ΔU_c over one cycle of the grid corresponds with ΔU_b, the voltage V_b can be periodically kept at a constant value.

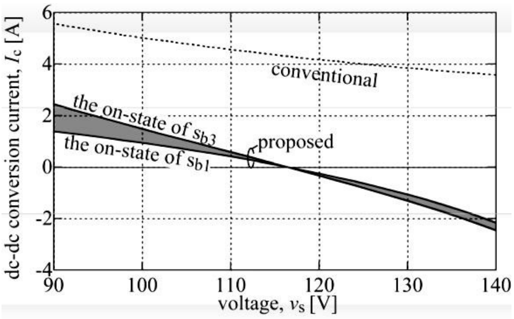

Fig 13. Dependence of dc–dc conversion current *Ic* on voltage *vs* with *Vg* = 100 V, *Io* = 5 A, *Lf*1 = *Lf*2 = 1.5 mH, and grid voltage frequency of 60 Hz

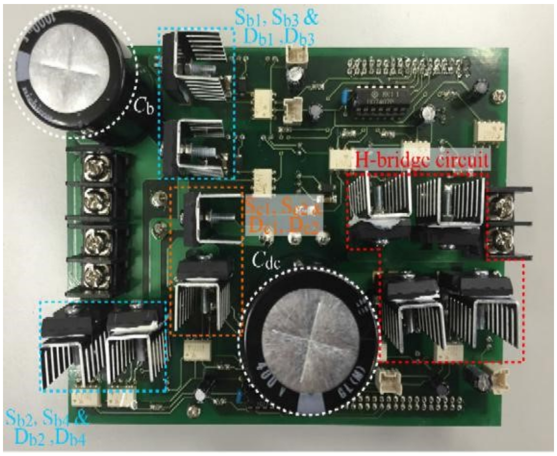

Fig 14. Test circuit

Circuit constants	Filter inductance ,*Lf*1 and *Lf*2	1.5mH
	Inductance L_c in dc-dc conversion circuit	2.5mH
	capacitance, *C*b and *C*dc	1.0mF

Table 3. Experimental Conditions

Fig. 13 shows the dc-dc conversion current I_c necessary to keep v_b at a constant value. The shaded area between the two curves is the possible range of I_c. One curve represents the results when s_{b1} is in the on-state and the other shows when s_{b3} is in the on-state. It is confirmed that the current I_c is zero at v_s = 117 V. At voltages below 117 V, the positive current charges C_b. In contrast, over 117 V, the current is negative, and the energy in C_b is transferred to the dc voltage source v_s by the circuit. The dotted curve in Fig. 13 represents the conversion current Is of the conventional inverter. The figure demonstrates that the current for the proposed inverter is smaller than that of the conventional inverter. This result implies that the inductor L_c in the proposed inverter can be downsized in comparison to that in the conventional inverter.

IV. EXPERIMENTS

Fig. 14 shows a test circuit of the proposed inverter. This test circuit can be changed to the conventional inverter by changing the connections. Therefore, comparison between the proposed and conventional inverters can be carried out because they use identical devices except for the capacitors as C_{dc} or the conventional inverter and C_b for the proposed inverter. Table 3 shows the experimental conditions.

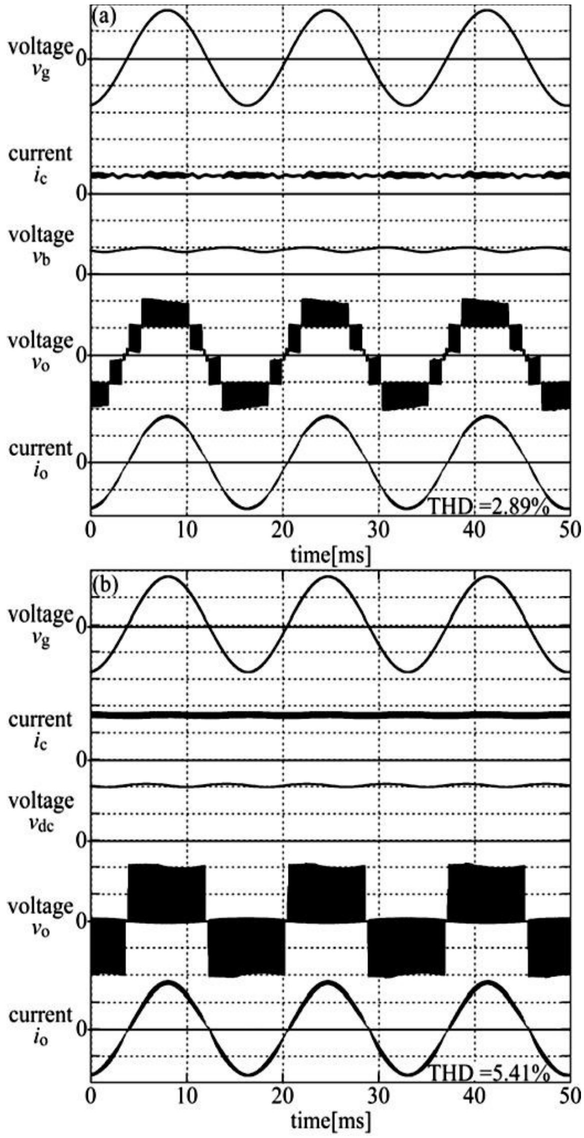

Fig 15. Waveforms for (a) proposed inverter and (b) conventional inverter during dc-c conversion under conditions of P_{ac} = 500 W, V_s = 90 V, V_b = 70 V and dc link command voltage V_{dcc} = 160 V. (The scales for v_g, v_b, v_{dc} and V_o are 80 V/div., and those for I_c and I_o are 4.0 A/div.)

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In terms of the proposed inverter, the conversion current I_c can be successfully controlled at a constant value and the voltage V_b can be maintained at a command value of 70 V. As a result, the proposed inverter can perform multilevel outputs in both dc-ac conversions. The current I_o of the proposed inverter achieves a smaller THD than that of the conventional inverter. The proposed inverter requires a filter inductance of 1.0 mH to obtain a THD of 5.0%. The conventional inverter, however, requires a filter inductance of 3.0 mH. Thus, the proposed inverter can reduce the filter inductance. Fig. 16 shows the efficiency of each inverter under various voltage conditions. The proposed inverter has a higher efficiency than the conventional inverter. Fig. 17 shows the power losses P_{Lb}, P_{Lc}, and P_{LH} in the energy buffer, dc-dc conversion and H-bridge circuits. The losses P_{Lc} and P_{LH} of the proposed inverter are smaller than those of the conventional inverter. The loss P_{Lb} is comparatively small. Fig. 18 shows the comparison between the detailed losses of the proposed and conventional inverters. Although the proposed inverter has larger conduction losses in the switches and diodes in total, the switching losses and the losses in the inductors are much smaller than those of the conventional inverter. Based on these results, the superiority of the efficiency of the proposed inverter is considered to occur because of the following factors:

1. The reduction of the current I_c through the chopper inductor L_c, which generates an energy loss because of the inner resistance of L_c.
2. The lower voltage applied to the switches and therefore the decreased switching loss. Therefore, the losses in the dc-dc conversion and the H-bridge circuits are reduced, and in particular, the loss of the H-bridge circuit is reduced to 18% in comparison to the conventional inverter.
3. The smaller ripple in the output current, which leads to a reduction in the iron loss in the filter inductors L_{f1} and L_{f2}.

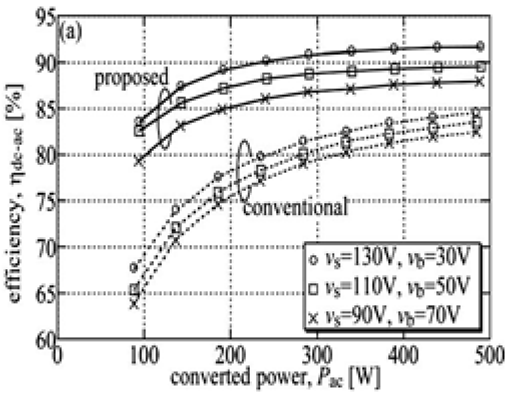

Fig 16. Efficiencies for dc-ac conversions

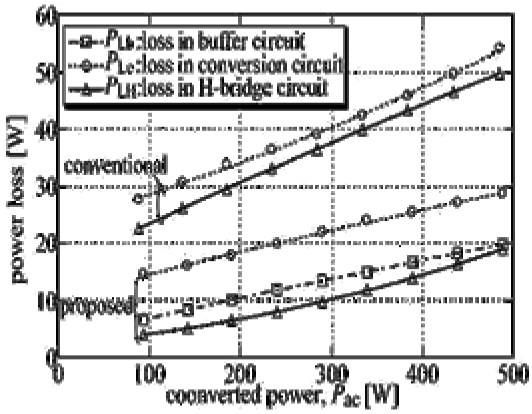

Fig 17. Power losses in each circuit during dc-ac conversion under conditions of v_s = 90 V, V_{bc} = 70 V and v_{dcc} = 160 V.

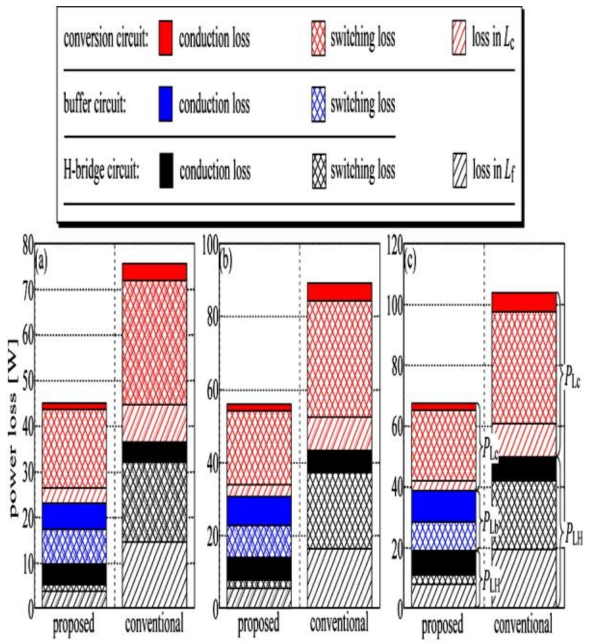

Fig 18. Comparison between detailed losses of the proposed and conventional inverters during dc-ac conversion of (a) P_{ac} = 300 W (b) P_{ac} = 400 W and (c) P_{ac} = 500 W under conditions of v_s = 90 V, v_{bc} = 70 V and v_{dcc} = 160 V.

V. VOLUME CONSIDERATION

Tables 4 and 5 give the voltages applied to the devices in the proposed and conventional inverters (refer to Appendix C). Considering that the voltages of v_s+v_b and v_{dc} nearly correspond with the amplitude of the grid, the switches in the H-bridge and the dc-dc conversion circuits in the proposed inverter require the same voltage rating as the switches in the conventional inverter. On the other hand, the applied voltage to the switches Sb1-Sb4 in the energy buffer circuit is low. Therefore, switches Sb1-Sb4 can be exchanged with switches with smaller volume. In the test circuit, MOSFET FMW30N60S1HF of Fuji Electric Co., Ltd., which has a voltage rating of 600 V, is used as the switch. For example, using the switch MOSFET FQP22N30 of Fairchild Semiconductor International, Inc, which has a voltage rating of 300 V, provides a 50% smaller volume. Furthermore, the heat sink attached to the switches in the proposed inverter can also be downsized in comparison to that for the conventional inverter, according to the measured loss shown in Fig. 17. If the required volume of the heat sink is, for simplicity, in proportion to the loss dissipated in the respective switches under an inverter output of 500W, the volume of the heat sinks used in the energy buffer, dc-dc conversion and H-bridge circuits in the proposed inverter can be reduced to 40%, 60% and 40%, respectively. In addition, the capacitor C_b satisfies a smaller voltage rating than C_{dc}. Therefore, the capacitor C_b can have a smaller volume than C_{dc} as shown in the test circuit. Although these in the test circuit have the same capacitance, the volume of C_b is 30% smaller than that of C_{dc}. Table 6 gives the estimated volume of these devices. The proposed inverter has a slightly smaller volume than the conventional inverter. Although this superiority may be canceled by the volume of the drive circuit for the switches, this consideration confirms that the volume increase caused by an increase in the number of the devices can be suppressed significantly.

	Applied Voltage
S1–S4	*v*s+*v*b
Sb1–Sb4	*v*b
Sc1and Sc2	*v*s+*v*b
*C*b	*v*b

Table 4. Voltage applied to devices in proposed inverter

	Applied Voltage
S1–S4	*v*dc
Sc1and Sc2	*v*dc
*C*dc	*V*dc

Table 5. Voltage applied to devices in conventional inverter.

VI. CONCLUSIONS

This paper proposed a new Three-phase inverter topology with an energy buffer circuit and a dc-dc conversion circuit, and described the control method for this proposed topology. The proposed inverter can output a multilevel voltage, which results in a decrease in the PWM harmonics in the output current. The proposed inverter can perform both dc-ac and ac-dc conversions with higher efficiency than a conventional inverter. The switches, the heat sinks attached to the switches and the capacitor used in the proposed inverter can all be downsized, because of the small applied voltage, and low loss dissipated in these devices. Furthermore, as a result of its multilevel output, the proposed inverter has a reduced filter inductance at the same THD. In addition, because of the reduction of the dc-dc conversion current, the chopper inductor can also be downsized. Consequently, the volume increase caused by the increase in the number of devices can be suppressed significantly. The proposed inverter is confirmed to be useful in practical applications.

APPENDIX A

Fig. A1 shows the simulated waveforms of the proposed inverter and the MEB inverter in [33]. The voltage v_b across the buffer capacitor of the MEB inverter pulsates with an amplitude level of 23V, which is over double the amplitude level of the proposed inverter. In addition, the current I_c through the inductor in the dc-dc conversion circuit of the MEB inverter has triple the magnitude of the that of the proposed inverter. This degrades the efficiency of the MEB inverter.

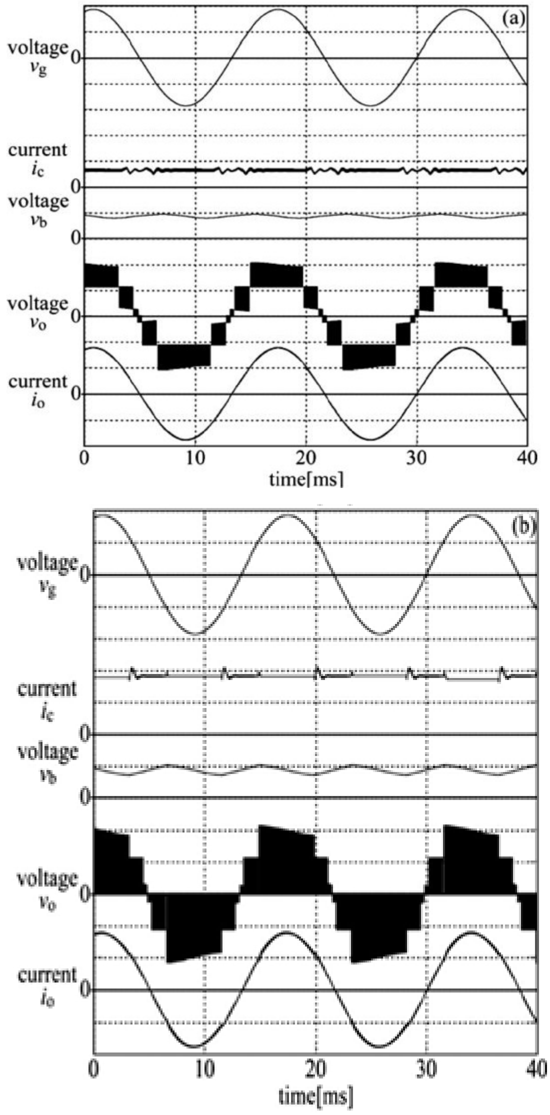

Fig A1. Simulated waveforms of (a) proposed inverter and (b) MEB inverter with a buffer capacitance of 1 mF during dc-ac conversion under conditions of P_{ac} = 500 W, v_s = 90 V and v_{dc} = 70 V.

		Conventional inverter			Proposed inverter		
		Volume per unit (mm^3)	number	Volume in subtotal (mm^3)	Volume per unit (mm^3)	number	Volume in subtotal (mm^3)
Switches	Buffer circuit		0	0	1300	4	5200
	dc-dc converter	3100	2	6200	1900	2	3800
	H-bridge circuit	3100	4	12400	1300	4	5200
Heat sinks	Buffer circuit		0	0	800	4	3200
	dc-dc converter	1700	2	3400	1700	2	3400
	H-bridge circuit	1700	4	6800	1700	4	6800
Capacitor		5500	1	5500	3800	1	3800
Total Volume				34300			31400

Table 6. Estimated Volume

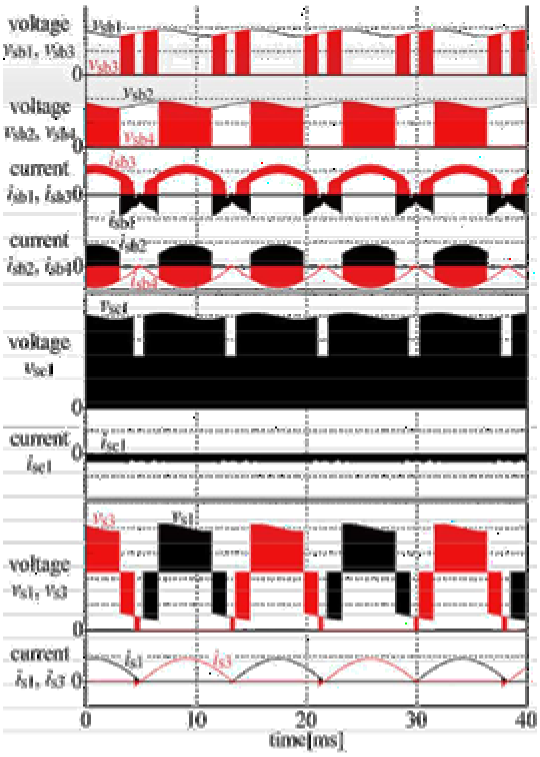

Fig A2. Simulated voltages and currents of the switches and the antiparallel diodes in proposed inverter under the simulation of Fig. A1(a).(The scales for the voltages are 40 V/div., and those for the currents are 8.0 A/div.)

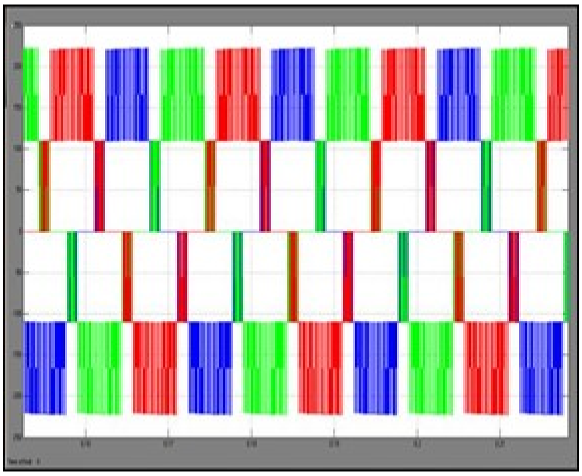

Fig 19. Simulated waveform for proposed 5-level three phase inverter

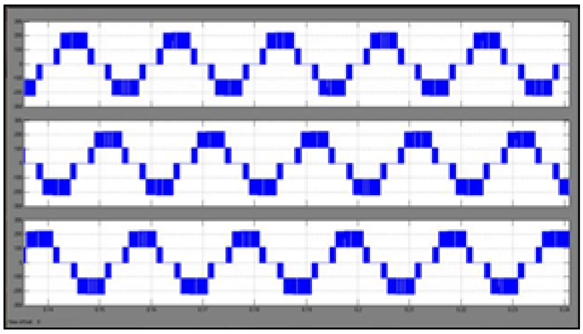

Fig 20. Simulated waveform for proposed 5-level Three phase inverter

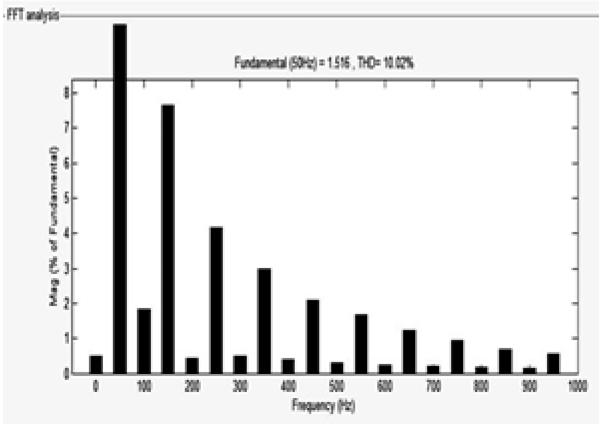

Fig 21. THD analysis for proposed three phase inverter

Fig 20 and 21 shows the simulated output waveform of proposed Three phase inverter. Fig 21 shows the THD analysis is of 10% which is less than that of convention inverter.

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