A Review of Decimating Filter Design for 5G Communication

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Abstract: One of the key components in 5G system is the baseband section, which consist of filter decimator unit, this module is called as decimating filter. Using this unit, the excess bandwidth can be removed, and the sampling frequency of the given signal can be reduced. The existing system works at higher frequency. As the power and frequency are directly related, the filter often tends to consume more power and the area consumption is also high. The main idea of this review is to discuss altering the architecture of the decimating filter such that the area and power consumption is reduced.

Keywords: Decimating filter; FIR; Decimator; 5G; Area; Power; Speed; Baseband; Communication system; Sampling frequency

I. INTRODUCTION

Communication systems consist of three main sections namely Radio Frequency (RF), Intermediate Frequency (IF) and a Base band (BB) section. RF amplifier is also called as low-noise amplifier (LNA). Its main function is to amplify the weak signal and therefore increase the sensitivity of the receiver without corrupting them with noise, so that the signal can stay above the noise level in coming stages. It must have a lower noise figure (NF). RF section includes frequency conversion module and RF front-end module. Radio Frequency and Intermediate Frequency section work with analog signals whereas base band section work with digital signals. Base band section consists of a decimating filter, demodulator and a decoder. Out of these three sections, this paper the mainly focused on the base band section which consist of a decimating filter which is a high frequency filter and a decimator combination. The high frequency filter generally used is the CIC (Cascaded Integrator-Comb) filter and FIR (Finite Impulse Response) along with the decimator. Research has been done to optimize this general filter-decimator configuration. Due to its high frequency working condition of this architecture, its power consumption is high (as power is directly proportional to Frequency, from the work-power equation Power=Work/Time and Time= 1/Frequency). The power utilization and area can be optimized by an efficient architecture, thereby improving the speed too. The main objective of this review would be to design an architecture that reduces the power and area requirement of the decimating filter. Consequently, the working speed of the decimating filter would increase. Thus, the proposed method is a further optimized one.

II. LITERATURE SURVEY

Wei Hu1, et al. [1] a multistage decimation filter architecture is designed to full fill the needs of commercial Analog to Digital Converter (ADC), the specifications along with the multi-objective optimization configuration. The multistage architecture combines the CIC filters, other filters to compensate and equiripple FIR filters at the different levels to better the performance. Gordana Jovanovic Dolecek, et al. [2] A simple method has been equipped for designing a comb-based decimating filter having larger aliasing rejection and a lower passband droop, by adding four extra unit zeros in the comb folding bands, where the aliasing occurs. Markeljan Fishta, et al. [3] This architecture sorts the drawback by using two serial peripheral interface (SPI) modules in a time-bound configuration. This method permits continuous acquisition and elaboration of comparatively higher speed digital signals. Divya Gautam, et al. [4] This technology designs a sample rate conversion filter for decimation, using the flat baseband, by which the complexity reduced by 50.5% and the pass band droop shows less than 0.007db in the proposed filter. David Ernesto Troncoso Romero et al. [5]. Mainly two changes have been performed, the first change is made by using Integrate-and-Dump (ID) block to perform decimation instead of the integrator-comb pair surrounding the down sampling register. The data-path is called CIC-ID. In the second change, the remaining comb filters is replaced with time-multiplexed-comb and the data-path is called CIC-ID-TMUX. Fabian Hqohn, et al.

[6] With the help of Remez exchange algorithm the decimating filter configuration can be further optimized in accordance with time delay. The computing cost is reduced by a multistage method and sparse filter design algorithm. Nithish Kumar V, et al. [7] MAC unit i.e., multiply and accumulate unit realized by the look ahead carry select adder and conventional adder modified the performance of the FIR filter. This is analyzed. The implemented FIR filter structure has length of 5-tap and 9-tap and HDL was used to develop this. SAED 90nm CMOS technology was used to implement this. V.Jayaprakasan, et al. [8] For WiMAX application the CIC based decimation filter has been realized by reducing the sampling rate at each section and also lowering the power consumed by enhancing the magnitude response and implementing it on the FPGA. Dejan N Milic, et al. [9] Modifications are made in selective multiplier-less CIC and FIR filter functionalities and it is us6ued in modern communication. Kamal Hossain, et a1. [10] In signal processing, in finite time the FIR filter becomes zero. FIR filters can be analogues or digital and it can be continuous or discrete in nature. Because of its lower area, cost, power, and higher operating speed the FIR filter is used in signal and image processing. S. M. Badave and A.S. Bhalchandra, et al. [11] Due to the use of multipliers the complexity of the FIR filter area increases. Among the FIR filter multiplier techniques, the most preferred one is the Distributed Arithmetic. In this technique, precomputed values of inner product are stored in due to its more efficiency. David J. Goodman, Michael J. Carey, et al. [12] In digital signal decimation and interpolation filtering is required. If there is substantial change in the rate, the process becomes more effective when the interpolation and decimation occurs in multistage rather than in single step. Eugene B. Hogenauer, et al. [13] A proposal of a class of digital hear phase FIR filters for interpolation and decimation is made. They do not require multipliers and use less storage making them more suitable for most of the applications. Ronald E, et al. [14] proposed a general theory for multistage interpolators and decimators for reducing the sampling rate. A set of necessary relations and curves for optimally designing multistage decimators is. Ankit given in the paper. Kurariya, et al. [15] A digital control system, interference when combined with the input signal, greatly influences the performance quality of the system. Therefore, the input signal should be processed to get the required signal. FIR filter is important in processing of digital signals. Bahram Rashidi, et a1. [16] here the active power utilization of digital FIR filter is brought down by using a considerably lower power multiplexer based on shift/add multiplier without clock pulse, it has been used on FIR filter till there was a reduction in power consumption. Abubakar Sadiq Hussaini, et al [17] wireless communication equipments are very big in size in order to fit in radio access technology (RATs) without an optimized design and fabrication technique. Shau-Ren Hung, et al. [18] have proposed an audio signal processing, majorly consisting of three sampling rates namely, 32 KHz, 44.1 KHz, and 48 KHz which are made use of in audio signal and image processing. It is essential to use multi rate signal processing methods to discard aliasing or imaging in latest digital signal processing techniques with varied input-output sampling rate. Hassan Fathabadi, et al. [19] For analog to digital conversion, the four proposed structures in the decimation filter are used. The Asymmetrical Digital Subscriber Line (ADSL) is present in the decimating filter, single multi rate IIR and FIR, three stage combination of FIR-FIR, combination of IIR-FIR, these are the proposed new configurations. Akshitha V Ramesh. et a1.[20] In Very-Large-Scale-Integration Technology, the Digital filters play a major role, in most of the VLSI systems addition is used as an integral operation, FIR filter is one amongst those, using adders the basic implementation of the filter is achieved. Vlastimir D. Pavlovic.0 et a1. [21] introduced a class of modified, selective, multiplierless CIC and FIR filter, whose usage is found in present day communication systems, it has high performance in comparison with the classical CIC filter. [22] Proposed a simple design method for Inter Symbol Interference (ISI) using a baseband filter. Cancellation of this is necessary in current mobile communication systems. Baolin HOU, et al. [23] A design methodology of parallel FIR filter, whose structure is parallelly transposed. Thus, the running speed has increased m times comparative with serial FIR filter, where m represents the given number of sub-filters, a very small delay is introduced by the FIR filter which are in parallel. Falah Hasan, et al. [24] the radio receiver is defined by the implementation of a programmable decimating filter that is to be utilized in the channelizer of multi-standard software. Shahana T. K, et a1. [25] The modern-day communication system requires higher capabilities like high data rates, discrete operating modes. This enhanced the growth of latest generation multi-standard designs of wireless transceivers. Tejal V. Rahate1, et al. [26] By using a filter which contains decimator unit which need a set of filters for listening device applications which gives sensible signal for the unquiet type of hearing loss. Using a different bandwidth filter, aid a person with hearing loss to pay attention and communicate by making sounds hearable and clearer.

III. METHODOLOGY

5G communication systems have transmitter and receiver sections as shown in Fig. 1 and Fig. 2. In this review, the receiver is considered. In 5G communication system, within the baseband section, the digital decimating filter performs functions like filtering of high frequency quantized noise and reduction of sampling frequency of the data to Nyquist sampling frequency. Thereby avoiding the requirement of analog reference circuits that have high precision and digital complex circuit that are high bit. The decimation filter performs anti-aliasing operation to keep the quantized noise from entering into the baseband section in the actual design process.

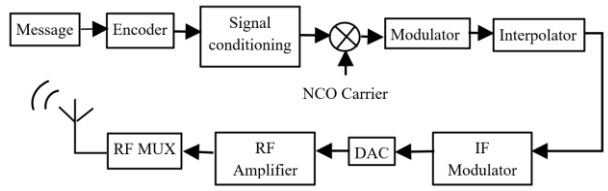

Fig 1. 5G System-Transmitter Section

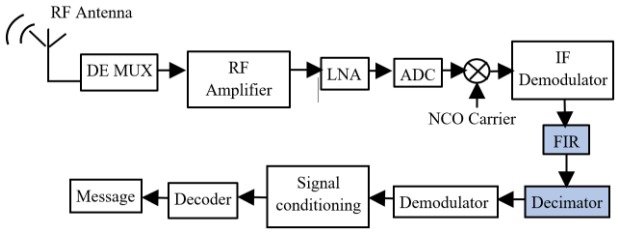

Fig 2. 5G System- Receiver Section

A. *Related work*

There are various methodologies to design a decimating filter. Some of them are discussed below. The traditional design of filter-decimator unit is as shown in Fig. 3.

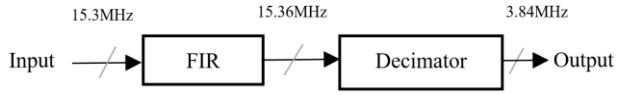

Fig 3. Filter-Decimator unit

Few multistage architectures combine CIC filters, other filters to compensate along with an equiripple implement FIR filter at different stages in order to balance the performance of the filter as a whole [1] [2] [4]. Some techniques that are proposed employs two SPI modules instead of CIC filter configuration, as this was found to facilitate elaboration of digital signals at a relatively high-speed and their continuous acquisition [3]. Several other techniques have been applied to other case studies and are practically realized. In one such technique, integrator-comb pair surrounding the down sampling register is being replaced by an Integrate and Dump block which performs decimation. The new data path formed is called CIC-ID path. And the remaining comb filters will be replaced with a time-multiplexed-comb configuration, and the new data-path is called CIC-ID-TMUX [5].

Reference [6] presents a filter-decimator combo design to perform integration of the signals with relatively high sampling rates. Consequently, signal sequences which has high or medium or low sampling rates are used based on the respective protection function requirements. The filter-decimator combo is optimized considering time delay and computational cost using a multistage approach and a suitable filter design algorithm. The most popular software implemented type of filters are FIR filters which performs filtering and also signal conditioning. Each of these functions accept input signal, blocks undesired frequency components, and then the original signal minus the undesired frequencies is passed as the output. Another research proposes the implementation of an efficient FIR filter configuration in terms of power and area using a modified Multiply and Accumulate unit i.e., MAC unit. The proposed FIR filter was implemented and its performance analysis is estimated with the MAC unit realized by the modified carry select adder and conventional adder [7]. Reference [8] has focused mainly on an efficient FPGA based design and realization of filter-decimator structure using CIC filters. Another review paper assessed the performances of several FIR design methods. Reference [9] proposes a modified multiplierless structure for CIC filters. The authors of another article have provided an overview of the latest trends and developments in FIR filter design methodologies in communication systems [10].

To illustrate the properties of the filter-decimator class a few design examples are reviewed in this article. Most of them used CIC filters and FIR filter combined. Some also used other complementary components. But there seemed to be more efficient approach than using a CIC filter or other complementary filters.

B. *Architecture of the proposed work*

An FIR filter is one which has a limited impulse response as it tends to settle to an absolute zero in finite interval of time. This is in contrast to IIR (Infinite Impulse Response) filters, as IIR filters might have feedback internally and might go on responding for an indefinite interval of time. A single-stage decimating filter unit design is being proposed as shown in Fig. 4, consisting of an FIR filter and a decimator unit.

Fig 4. Proposed Decimating Filter

A low pass filter is used for FIR filter here. This single-stage filter-decimator combo must be designed to remove harmonics present in the signal and also avoid aliasing. The FIR filter must be realized using direct form FIR architecture. The decimator must pick every Nth sample, ignoring other samples, where N is its decimating factor. The FIR architecture and decimator is to be developed and implemented on an FPGA. The final receiver section would like Fig. 5.

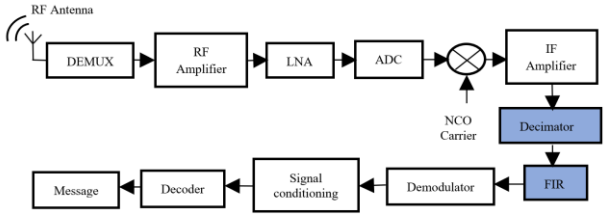

Fig 5. Proposed 5G System- Receiver Section

But the challenge in following this method would be to avoid aliasing as mentioned earlier and also to avoid signal loss, as decimation of the signal samples are performed first and then the filtering. So, the new architecture must be developed in such a way that the efficiency of the filter-decimator combo must not be compromised.

IV. CONCLUSION

From all the research work that was referred, most of them have used a configuration of CIC filter along with FIR filter. Some have also used other complementary units like SPI modules or other modified CIC structure. A much simpler and effective architecture is being proposed using a single-stage decimating filter unit. The architecture is to be designed in such a way that aliasing is avoided and signal loss is minimized, but at the same time, the efficiency is not compromised. Performing the decimation first and then the filtering is being proposed here, with an efficient design to avoid the above-mentioned issues.

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