A Survey on VLSI Implementation of Low Power, High Speed DAC

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Abstract: Digital to analog converters, are commonly used to convert digital data streams into analog audio signals, this conversion is important because it significantly increases the overall value of the system. There are many strategies that are already developed in the DAC (Digital to Analog) converter field to meet necessary requirements. The Low power Current Steering 6-bit counter and R-2R ladder Digital to Analog Converter are designed in this paper. In this the R-2R ladder network is designed using only two Valued resistor R and 2R the switch is designed using NMOS and PMOS Transistors. This design is operated with low voltage by using DTMOS logic. This design aims to achieve less INL (integrated nonlinearity) of 0.3 and DNL(differential nonlinearity) of 0.06. It consumes only 1V of power and it requires 10Ghz frequency. This entire DAC design is operated with the help of 180nm CMOS technique.

Keywords: DAC, R2R, Low Power; Current Steering; CMOS

I. INTRODUCTION

The data or the information that perceived is analog form while the digital devices such as cellphone, calculator can only process the data signal in digital form. Analog to digital Converter (ADCs) and Digital to Analog Converter (DACs) are the two types of converters that are commonly used in all real time systems. The Digital to Analog converter (DAC) with high sampling rate, medium resolution is more and more required for high speed data links such as optical communication systems, satellite communication systems and very advanced application of Digital to Analog Converters with low power, high speed 5G mobile communication systems. In this work gives implementation of Low power, high speed DAC using VLSI cadence software. The R-2R ladder architecture gives architecture appropriate for strategies, which is applied by using highly linear resistors. Those DACs encompass a shape of resistors, that is having values may be closely matched. This topology is binary weighted and may provide a better resolution as compared to its in simple terms binary weighted counterpart. a completely popular architecture for D/A converters are R-2R ladders. The R-2R ladder structure is suggested below.

II. LITERATURE SURVEY

B. Razavi et.al.[1]. In this paper, a new 10-bit hybrid DAC by combination the current sources and resistor ladder has been presented. The power consumption for simulated DAC is just 8.4mW in 1.2V power supply and 1.2 GHz clock frequency. Lucas Duncan et.al.[2]. This work narrates relaxation digital-to-analog conversion technique, which takes advantages of exponential impulse response of a first-order RC network to generate binary-weighted voltages. The proposed to design standard cell based, mismatch-insensitive, ultra-low power.

Tsung-Ming Chen et.al.[3]. This paper presents a static and dynamic errors including current source matching errors are eliminated by optimization of floorplan and layout aiming to minimize power consumption. Jim Geier [4]. This paper explains the 10-bit 400kS/s and a 10-bit-2MS/s Relaxation

Digital to Analog Converters (ReDAC) in 40nm are presented in this paper. B R Greenley et.al [5]. This paper gives an insight to the design of DAC which will be used in different types of ADC's. Congyi Zhu et.al [6]. This paper represents a mixture of various signals to detect the time violations of the high speed and high resolution analog clocks. R J Van de Plassche [7]. This paper presents In low power networks DACs are the essential elements and it consumes a more power, this paper presents a new less power DAC.B Razavi. [8]. A 14nm FinFET CMOS 12-bit current-steering digital-to-analog converter (DAC) for 2G/3G/4G mobile applications Plassche R. et.al.[9]. This paper presents the newly proposed DAC is to achieve low power utilization. Mamun Bin Ibne Reaz et.al [10]. Main aim of this paper is utilization of low power depending on a current routing design in the presence of an amplifier Amirhossein Ahmadi et.al [11]. This paper presents a Static and dynamic errors including current source matching errors are eliminated by optimization of floorplan. Jakub

Dalecki et.al [12]. In this paper 3rd-order dual truncation multistage noise shaping technology, SFDR of 110dB and SNR of 115dB is achieved and it its measured harmonics are all below -110dB.

III. METHODOLOGY

Digital to Analog Converter (DAC) is integrated the devices to convert a digital signal to analog signal with excellent resolution, low power consumption, small chip area, and high-swing is needed. A DAC can be implemented in three main methods: resistor ladder, resistor ladder and current steering, switched capacitor. The proposed work uses the method of resistor ladder and current steering for low power consumption by utilizing switching component explained in the next section.

A. Related Work

There is various methodology to design a DAC, some methods are discussed below: In spite of simplicity in implementation and good matching, resistor and capacitor DACs aren't suited for high frequency and high resolution applications. Thus, current steering DACs are more suitable choices for the aforementioned applications due to their high speed and proper accuracy implementation capability. Current steering DACs are divided into three categories: binary-weighted, unitary, and segmented. In binary weighted structures, the number of current sources is equal to the number of bits and the current of each source is twice the previous one. Simplicity and speed are its advantages but enough accuracy and good matching, especially in high resolution, are difficult to achieve. The below method is more efficient as it as low power consumption, high speed.

B. Architecture Of Proposed Work

In this new method, the binary weighted and unit current sources are combined with a resistor ladder to reduce the power dissipation and the number of current sources. This method improves the dynamic and static characteristics. DAC which consumed 8.4 mW power with a 1.2 V power supply can be estimated to reduce to 1.5mw.

The proposed design is developed by using CMOS technology with180nm. Here the resistive circuit is designed by using poly resistors. The first rate gain with the proposed DAC is the so called R/2R DAC, which uses fewer precise resistor values. Manufacture can be simplified if there are fewer one of a kind resistors value to make. At the output node of the switches having the same low resistive load. When we are looking from the output can observe that the input impedance is always 2R. At the leftmost slice the impedance is given by two resistors in series and the input impedance is 2R. At the next section the same applies since we have a 2R resistance in parallel with the two series R resistances.

The contemporary resources are assumed to have infinite output impedance. Ultimately, the output impedance of the overall DAC is 2R. a very popular architecture for virtual to Analog Converters is R-2R ladders. These R-2R ladders are very helpful for understanding binary weighted currents by using only R and 2R not depending on the number of bits. As an end result, this R-2R technique typically gives each a smaller length and better accuracy than different procedures. Fig 1 shows the proposed block diagram for DAC.

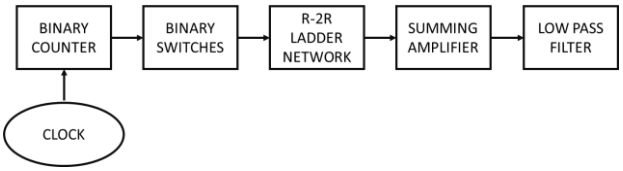

Fig 1. Proposed block diagram of DAC

The 6-Bit counters get the digital data from the sensors and output of that is applied as input for the binary switches. The Binary Switches consists of NMOS and PMOS transistors and is controlled by input binary data. Terminal voltages of R-2R ladder is changed accordingly and resulting output voltage is found using the equation,

$$V_{out} = -V_{ref} \sum_{i=0}^{n} b_i \frac{1}{2^{i+1}} \quad \text{….. (1)}$$

The obtained output voltage is amplified using summing amplifier.

The amplified voltage signal is passed through low pass filter to get smoothened signal.

Thus, 6-Bit binary input data is converted into analog data. The block diagram of proposed architecture is explained as follows.

a) *Counter*: The counter consists of six stages with cascaded D- flip-flops as shown in Fig.1. Only one flip-flop is connected to clock and other is clocked by previous flip flop output. Reset is connected to all the flipflops. When the least significant bit undergoes transition then the information will be rippled through all the D-flipflops. The output of first flip-flop is given as clock input to the second flipflop and so on up to sixth D-flipflop. Since it contains 6 bits therefore it generates up to 64 states. The output of ripple counter is acts as input to the binary switches of R-2R ladder. The design of 6-bit asynchronous counter is utilized.

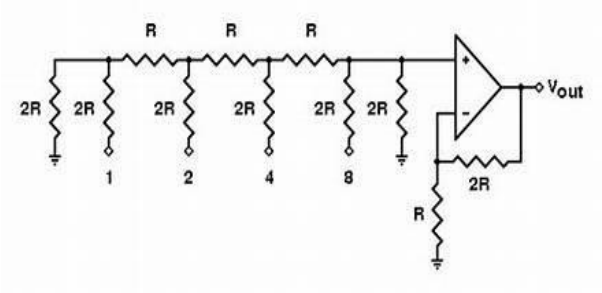

Fig 2. R-2R Ladder Network

b) *Binary Switches*: The digital input control the switches and connect an input either to a common voltage V or to a virtual ground of an op-amp. Binary switches are shown in Fig 3.

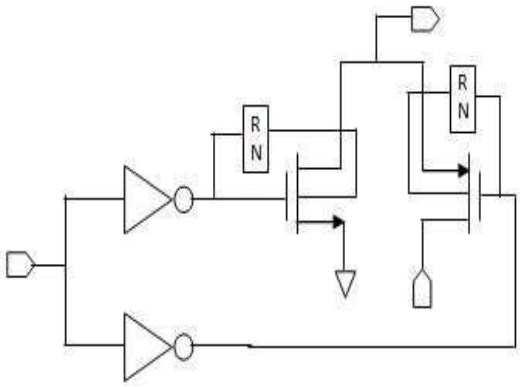

Fig 3. Circuit diagram of binary switch

c) *Summing Amplifier*: In this project op-amp is used as summing amplifier.

d) Low-pass Filter: It is used to obtain distortion less analog wave at the output.

e) R-2R Ladder Network: This arrangement uses resistors of only two different values of ratio 2:1. The resistor value used are R=3KΩ, 2R=6KΩ, R_f=3KΩ.

C. To study the working of R-2R DAC.

The topology is binary weighted and provide a high resolution compared to its purely binary weighted counterpart. A very popular architecture for D/A converters uses R-2R ladders. Fig 2 shows the R-2R ladder DAC. The resistor value used are R=3K, 2R =6K, Rf=3K.These ladders are useful for realizing binary weighted currents with a small number of components and with a resistance ratio of only 2, independent of the number of bits N.

IV. CONCLUSION

Digital to analog conversion is a process which is often required for application such as radar, satellite communication, wireless applications. The design process of 6-Bit 10 GS/s binary weighted DAC includes the realization of individual blocks such as Binary switches, R-2R ladder network, summing amplifier, low pass filter,6-bit counter and parameters like low power high speed, less area have been optimized. This design achieves less INL and DNL of 0.3 and 0.06 respectively. Therefore, we can conclude that VLSI implementation of low power, high speed DAC system is better for getting accurate results.

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