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A 5G Based Demodulator On FPGA

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Abstract: In a digital communication system, demodulation is one of the key components. Often, during demodulation the problem of phase error arises, which has to be detected and corrected in order to get the right information. A phase locked loop is employed for the same. A BPSK modulation technique is used for modulating message signals in a 5G environment. The idea of the paper would be to develop a phase error detection & correction system, aiming at a low power & low area architecture. Both proposed and existing systems are implemented in Spartan 3E FPGA. Simulation is done in VHDL using Xilinx and MATLAB software.

Keywords: Demodulation; Phase error; Phase locked loop; 5G; BPSK modulation

I. INTRODUCTION

Modulation is the process of changing one or more features of a periodic waveform, called the carrier signal, with a modulating signal that often carries information to be transferred . We can deliver a signal over a bandpass frequency range via modulation and also we can broadcast many signals concurrently if each signal has its own frequency range. Phase inaccuracy in the received signal can lead to erroneous demodulation. During data transmission or reception some unwanted signal get introduces into the communication system, which decreases the quality of the receiver. Such induced disturbance termed as "Noise". This noise causes the problem of phase error during demodulation, which has to be detected and corrected in order to get the original data back. Phase error mitigation is achieved via a Phase Locked Loop (PLL). The idea of the paper would be to develop a phase error detection & correction system, aiming at a low power & low area architecture. That is increase the efficiency in terms of power and area utilization on hardware of the internal components of the Costas loop/PLL such as FIR filters and NCO's for 5G specifications. According to the 5G specifications of 3GPP company, Binary Phase Shift Keying (BPSK) is proposed as the modulation technique as it provides better signal coverage compared to other techniques of phase shift keying such as QPSK. BPSK is believed to be a strong modulation method since its receiving mechanism is simple to remember. In comparison to QPSK, BPSK allows for a greater distance between the base station and mobile users. Although when QPSK is used, more bits are transmitted than BPSK but QPSK is more error-prone.

II. LITERATURE REVIEW

The main aim of the paper[1] is to develop a hardware module for IEEE802.15.4/Zigbee devices which is BPSK MODEM for 868MHZ band. In this paper they have designed an energy scalable Zigbee system on a system on chip by integrating all operational functions on one single This algorithm provides an iterative method for vector rotation by using only shift and adds by arbitrary angles. silicon die in order to improve performance, cost, time to market. In paper [2] implementation of digital modulation techniques BPSK and QPSK on Spartan 3E-Field Programmable Gate Array (FPGA) using Verilog Hardware Description Language (VHDL) is done. Here they have proposed two modulation methods for BPSK/QPSK. The proposed method one uses direct digital synthesizer as IP. Whereas proposed method 2 uses ROM for main storage of data in order to produce the same BPSK/QPSK signal hence it does not require multiplier, adder & subtractor. The proposed modulator method 1 utilized less area compared to proposed modulator method 2. In paper[3] carrier recovery scheme using simple trigonometric functions is developed. The carrier Synchronization is one the major issue in the communication systems. The proposed carrier recovery scheme can recover any frequency and phase offset in the carrier of the transmitter end. This carrier recovery scheme uses trigonometric functions for protocols that carries the harmonics of the pilot which does not require parameter tuning like conventional carrier recovery schemes such as Phase locked-loop or Costas loop. The proposed scheme is easily implementable on modern digital hardware compared to conventional one and it can also be implementable on Software Defined Radio's (SDR's). In Paper[4] new approaches for BPSK modulators are recorded and compared with the conventional BPSK modulators. The BPSK modulator using Booth Multiplier and proposed BPSK Modulator-3 utilizes less power compared to conventional BPSK method also the area and device utilization is reduced compare to the conventional method. In paper[5] Costas loop is designed for carrier recovery mechanism of BPSK modulation by using certain mathematical models and digital design of Low Pass Filter (LPF), Loop Filter (LF), Voltage Control Oscillator (VCO), Phase Detector (PD) and the multiplier are simulated and integrated in Xilinx using VHDL. In

paper[6] a novel quadrature tracking demodulator is developed for LTE-A applications in order to coherently demodulating the orthogonal frequency division multiplexing (OFDM) signals. It can effectively demodulate an 18Mbps signal of LTE-A with a quadrature imbalance up to 15 degrees. Paper[7] detailed about the CORDIC (Co-ordinate Rotation Digital Computer) algorithm working and its implementation using FPGAs. The DSP microprocessors are cost effective, offers greater flexibility but they usually operate at low speed. The advanced reconfigurable logic computers can operate at high speed. But the algorithm developed for these microprocessor-based systems do not map into well hardware. Then CORDIC algorithm came into picture. CORDIC is a set of shift and rotation algorithm for computing wide range of functions which includes trigonometric, hyperbolic, linear and logarithmic functions.

III. BLOCK DIAGRAM OF COSTAS LOOP

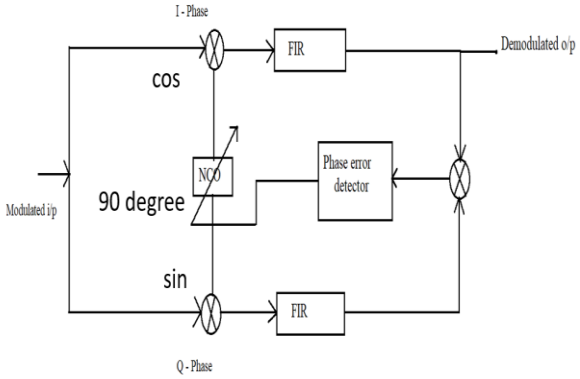

Fig 1. Block diagram of Costas Loop.

The above Fig.1 shows the Costas loop architecture. The input signal is divided into in-phase and quadrature-phase. Both signals are multiplied with sinusoidal carrier, with a 90-degree phase shift between two oscillator outputs. The numerically controlled oscillator (NCO) generates the required carrier signals. The product of modulated signals of I-phase and Q-phases with NCO outputs are filtered using identical filters, these filter signals are multiplied and the product is fed to the phase error detector module that eventually corrects NCO's signals to eliminate the phase error. This is performed by synchronizing the NCO outputs with the input signal.

A. LUT BASED NCO

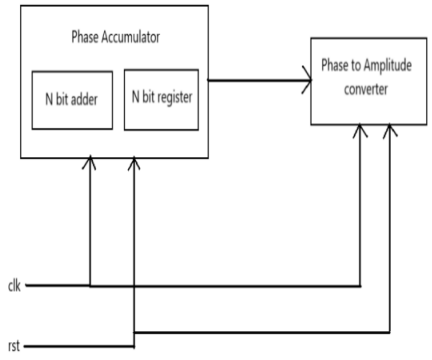

Fig 2. Numerically-controlled oscillator

The LUT based NCO architecture shown in figure 2. It consists of a phase accumulator (PA) and a phase to amplitude converter (PAC). Figure 6.9 shows the LUT based NCO architecture. The PA consists of N bit adder and N bit register. Whenever the sum of the absolute values of its operands is greater than its capacity i.e., $2\,N-1$ then the adder overflows. As a result, the output word width always equals the input word width and the overflow bit is neglected. The remainder value is recorded in the register. The output of PA is given as a input to PAC block. In PAC sine and cosine values are precalculated and stored in the form of array which generates sine and cosine amplitudes. The major drawback of LUT based NCO is it can used for only fixed frequencies.

B. FIR FILTERS

For the FIR filters cutoff frequency, stop band and pass band frequencies are calculated.

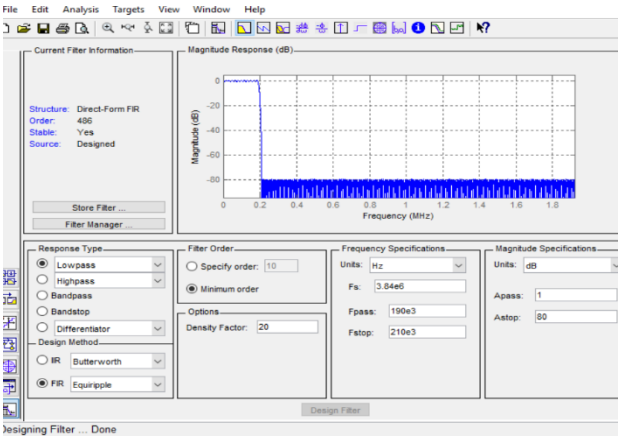

Fig 3. Filter Design Analysis Tool

The filter coefficients are calculated from Filter Design Analysis (FDA) tool using MATLAB for all these frequencies. fcutoff=200KHz, fpass=190KHz, fstop=210KHz. Obtained order =486 from FDA tool. The filter design analysis is shown in Fig. 3.

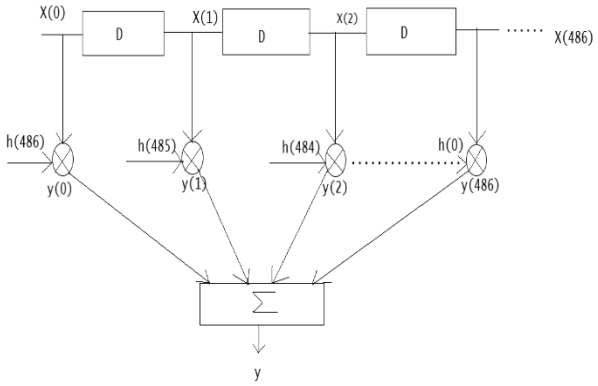

Fig 4. Logic block architecture of the existing FIR filter

The Fig. 4 shows the logic lock architecture of the existing FIR filter. The variable x(k) refers to the nth input sample, e.g., x (2) refers to tap number 2. The variable h(k) refers to the nth coefficient of the FIR filter e.g., h (2) refers to coefficient 2 and 'D' is the delay elements of the filter. The equation for this filter is given by

$$\mathbf{Y(n)= \sum_{k=0}^{486} x(k)h(n-k)} \quad \text{-------(4)}$$

C. FPGA MODULE

In FPGA module the receiver part of the code in embedded within the JTAG block. The phase error to be added in the channel can be given using the phase error constant block. The transmitter and channel blocks contain the transmitter and channel MATLAB codes, called ads functions. To verify the result, the mean of the error is displayed. Based on the mean value occurred the phase error can be estimated. Finally, the demodulated output is exported to workspace of MATLAB, where it could be plotted and the result can be visualized.

IV. RESULTS AND DISCUSSIONS

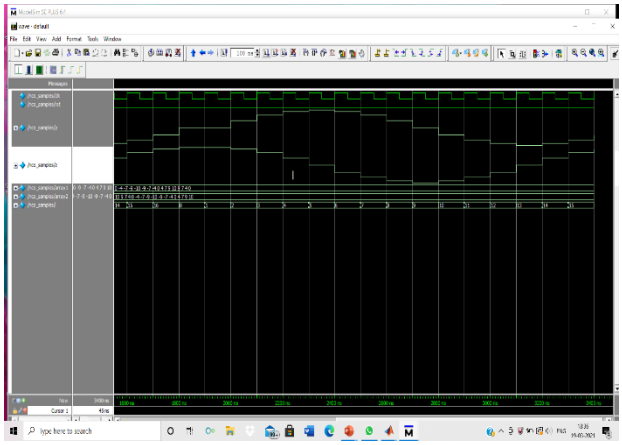

Fig 5. LUT based NCO output waveform.

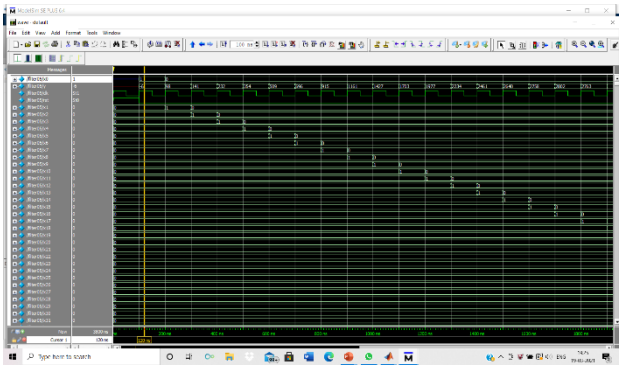

Fig 6. Impulse response of the existing FIR filter.

	Area Utlization (%)	Timing Utilization (ns)	Power Utilization (KW)
LUT based NCO	0.4493	3.983	0.78
Existing FIR filter	55	5.177	75.98
Total	55.44	9.16	76.76

Table 1. Area, Timing and Power utilization of existing and proposed oscillators and filters.

The LUT based NCO has utilized 0.4493% of area, 0.78KW of power and its input arrival timing utilization is 3.983ns. For fm=24KHz, fc=240KHz, and fs=3.84MHz we got only 17 samples for LUT based NCO, in case if we increase any of these frequencies then it occupies large area, power and works at lower speed. LUT based NCO are used for fixed frequencies. The FIR filter has utilized 53% area from the total available area, 75.98KW power and its input arrival timing utilization is 5.177ns.

V. CONCLUSION

The Costas loop circuit has been developed on FPGA and its area, power and speed values are calculated. Its working has been verified in both time as well as frequency domains. This design can be implemented to perform demodulation in 5G system to tackle the problem of phase error.

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