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Digital Down Converter for 5G systems

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Abstract: Current trending research in the field of VLSI and communication is development of architectures for 5G systems. The architectures developed not only have to be compatible with the proposed standards by 3GPP, but also must be efficient in terms of its operations. One of the major units of a 5G receiver is a Digital Down Converter. This unit is responsible for converting the intermediate frequency to baseband frequency. This paper summarises few recent advancements made in this regard.

Keywords: Digital Down Converter; 5G; Communication; Survey

I. INTRODUCTION

5G is the fifth-generation technology standard for the broadband cellular networks. It is designed to increase the speed, reduce latency, and improve the flexibility of the wireless devices.5G uses higher radio frequencies that are less cluttered. This allows for it to carry more information at a much faster rate.

A communication system consists of an RF, an IF and a baseband section. The baseband section involves conversion of IF to baseband frequency, demodulation and decoder modules.

The module that converts IF to baseband is called Digital Down Converter (DDC) and by using this the input signal is reduced to a lower sampling rate, thus it allows lower-speed processors to process incoming fast signals. The DDC performs the fundamental function in communication systems and is used in radio receivers. It is implemented with the aid of field-programmable gate arrays or application-specific integrated circuits.

The main goal of this work would be to reduce area and power consumption of DDC to increase the overall efficiency of the baseband section by changing the architectures of filters and oscillator involved.

In this paper, we modify the architecture of FIR filter such that lesser multipliers and adders are used. Finally, simulation results are illustrated and the power, area and speed values for both existing and proposed architecture are calculated.

II. LITERATURE SURVEY

A. *"Digital Up and Down Converter for High Performance VHF and UHF Transceiver" by Pavel Ková , Pavel Puri er, Tomáš Morong*

The proposed architecture of transceiver uses digital design of the receiver and transmitter intermediate stage. The implementation of the transceiver by digital intermediate frequency stages (DUC/DDC) brings new quality to the professional transceivers which enables to minimize implementation losses compared to analog systems. The advantage of using DUC and DDC are unmatched quality of modulation signal and good manufacture repeatability, a receiver can be implemented without linear distortion of the processed signals respectively. The modulated signal quality is better than at the transceivers with classical analog angular modulators.

The drawback of the proposed digital design could be higher power consumption as compared to the analog system because of the passive filters used and also the use of an A/D and D/A converter limits the performance.

B. *"Filter Analysis in the Quadratic DDC Structure" by Guo Lianping, Meng Jie, Tan Feng*

This paper presents a quadratic Digital Down-Conversion (DDC) structure which moves Intermediate Frequency (IF) signal to baseband by two steps. Firstly, IF signal is passed to baseband nearby using a structure based on polyphase filter. This structure places mixers after polyphase filters. Then, the signal is passed to baseband through conventional orthogonal frequency mixing. This architecture can reduce filter resources and effectively reduce the sample rate and process cost by improving the operation efficiency. Also, this paper analyses the way of implementing the complex coefficient filters resulting from the prepositive filter structure.

However, the digital filter with complex coefficients is introduced with the quadratic DDC structure, which

makes the quadratic structure difficult to implement on FPGA to some extent.

C. "IF Waveform Generation and Digital Down Converter with RTIO Board" by Nazhat Salma M, Prathiba,Shanbog

The radar system consists of a transmitter and a receiver, where the transmitter reflects from the object and returns to receiver with some information about an object. All the received signals from the receiver should be pre-processed prior sending it to the signal Processing stages. Here DDC is used for pre-processing the signal. The disadvantages of DDC using single stage FIR filter are made to overcome using Multistage FIR filter approach, which is more efficient. The main aim of the proposed methodology would be to implement the DDC on FPGA (Virtex-5) which as advantages in areas of hardware complexity, speed and power dissipation.

The downside of this proposed system will be the area penalty for field programmability and expensive production volume FPGA.

D. "A Polyphase Digital Down Converter Method for GHz High Speed Sampling Signal" by Zhao Kongrui, Zhang Chao

In this polyphase digital down-conversion method, the high-speed sampling input signal and the oscillation signal are parallelized, then to decrease the speed of the incoming signal, the input signal is decomposed to M sub-channel by polyphase decomposition. The digital down-conversion operation is executed for every channel of input signal data and by the poly phase filtering, down-conversion of the high-speed sampling signal can be carried out at low sampling speed signal. Later the simulations are performed to check the efficacy of this method.

The disadvantage of using polyphase digital down-conversion method is, it requires a large amount of hardware resources

III. PROPOSED METHODOLOGY

The architectural block diagram of DDC is shown in Fig. 1. To make the design efficient individual architectures such as NCO and FIR circuits must be modified.

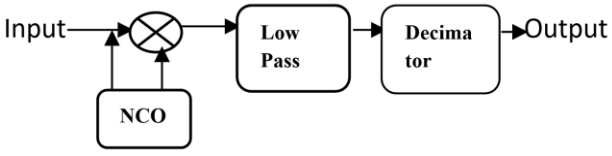

Fig 1. Architectural block diagram of DDC

IV. CONCLUSION

In this paper, new architectures of filters and oscillator are explored. The filter architecture is modified which results in the reduced number of filter co-efficient which in turn reduces area and power consumption. Using the proposed system, we will be overcoming the drawbacks discussed in the literature survey and also the speed and efficiency of the system are increased.

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