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Digital Down Converter For 5G Systems

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Abstract: ***The high data rate message signals in 5G communication system is difficult to process the signals. Implementation of DDC in 5G systems is a better solution. The efficient way of designing and implementing a Wideband Digital down converter has been discussed. Since the received signal is RF signal of high data rates, intermediate frequency (IF) stage is used. The message signal is sampled and given as input as input to DDC. Sinusoidal signal generator based on CORDIC is used to demodulate the IF baseband signal. It is shown that filter bandwidth varies by decimation factor. Filtering is implemented in stages to obtain efficient response. Decimation by 4 and decimation by 2 is used after first FIR filter and next FIR filter respectively. MATLAB R2011b, ModelSim SE-6.4, Xilinx 13.2 version is used to simulate each block of DDC at system level testing and Sparten-3e FPGA hardware used implementing the design.***

Keywords: CORDIC; FPGA; NCO; VCO

I. INTRODUCTION

Communication means the exchange of information between two or more individuals. Wireless communication is the exchange of information between two or more points that are not connected physically or by an electrical conductor. There are different modes of communication at this juncture of modern Digital Communication. The transfer of signals are in digital format i.e., bits. Any communication system consists of a transmitter at the source of the message signal, a channel and a receiver at the destination. The DDC presented in this paper is the key component of Receiver. The frequency band of interest is downscaled to baseband signal. The RF signal is downscaled to baseband signal to easily retrieve the message.

II. LITERATURE REVIEW

Digital Down Conversion involves the process of the shifting a high rated signal to a standard signal. The message signal at the receiver is a wide band signal with noise signal. For the end user only message signal is required which is a small portion of the entire band. The DDC operations include filtering and decimation of a received message signal which makes the downscaling process easier.

A. CORDIC Algorithm

The CORDIC (Coordinate Rotation Digital Computer) was developed by Jack Volder in 1959. It is an iterative algorithm to convert between polar co-ordinates to cartesian co-ordinates or vice-versa using shift, add or shift subtract operations respectively. It can also be used to compute trigonometric functions such as sine, cosine, polar to rectangular coordinates etc. In this design arithmetic shift is used instead of logical shift.

Consider '1100' after logical right shift becomes '0011' where the blank bits from LSB are filled with zeros. Similarly, '1100' after arithmetic right shift becomes '1111' the blank bits from LSB are filled with MSBs.

As the number of iterations varies from zero to infinity the product approaches numerical value 0.6073. The desired rotation angle say $\theta = \pi/6$ or any is initialized to angle accumulator. In the rotation mode the rotation decision at every iteration is made for diminishing or minimizing the magnitude of the residual angle in the angle accumulator. The rotation decision of every iteration is hence based on residual angle sign after each step in the elementary operation. The CORDIC equations used for rotation mode are,

$$x_{i+1} = x_i - y_i * d_i * 2^{-i} \quad (1)$$

$$y_{i+1} = y_i + x_i * d_i * 2^{-i} \quad (2)$$

$$z_{i+1} = z_i - d_i * \tan^{-1}(2^{-i}) \quad (3)$$

where, if $z_i > \theta$, $d_i = +1$, else $d_i = -1$.

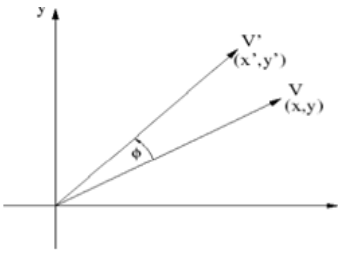

Fig 1. Rotation of a vector V by angle θ

B. Digital Up Converter

In the transmitter of a communication system a Digital Up converter is implemented. The message signal from the source is interpolated i.e., the desired number of insignificant extra samples are added for the message signal samples. If the sampling frequency is low then

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Gaussian noise is generated, which is responsible for tampering of IF and baseband signal. This leads to weaken the message signal strength. Similarly, if the sampling frequency is high then the message signal strength is increased, further we cannot manipulate the samples of the message signal.

At Nyquist rate of sampling to enhance the signal strength and signal characteristic we interpolate the message signal by the interpolation factor 'L'. The decimation factor 'M' in the down converter should match the interpolation factor preferably 2^n (2 power n) where n is the number of bits used to represent the message signal sample.

III. DDC ARCHITECURE

A Digital Down Converter consist of four basic blocks:

a) Local Oscillator using CORDIC (Coordinate Rotation by Digital Computer)

b) Mixer

c) FIR filter (Finite Impulse Response) filter

d) Decimator

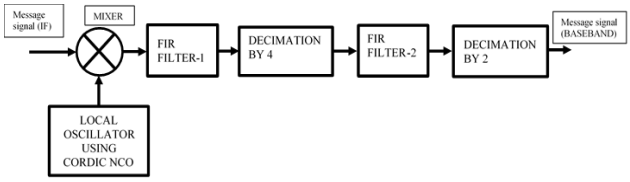

Fig 2. Block Diagram of Digital Down Converter

A. *Local Oscillator using CORDIC NCO*

Oscillators in communication will generate local reference signal of specific frequency. They are widely used in modern communication circuits which includes filters, modulators, demodulators and also forms the basis of frequency synthesizer. Oscillators attribute accurate time measurement and co-ordination in the important stage of communication systems. They are used to stabilize time in frequency generators. Oscillators also provide carrier signals and pilot signals for electronic communication and navigation.

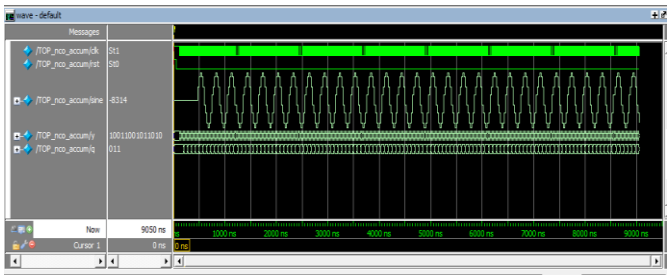

Fig 3. Output of NCO using CORDIC

Oscillators can be realized in both analog and digital forms. Voltage Controlled Oscillator (VCO) is an analog frequency generator, where the output frequency is adjusted by changing the values of passive components in the circuit and input voltage to the circuit. VCO is used for frequency modulation, phase modulation and in PLL. On the other hand, Numerically Controlled Oscillators (NCO) are digital frequency generators. These are often used to generate sinusoidal, triangular or rectangular periodic signals in discrete form.

B. *Mixer*

Intermediate signal demodulation involves multiplication of message signal with the oscillator signal from local oscillator i.e., NCO using CORDIC algorithm.

C. *FIR Filter*

Based on the response theory of linear system the digital filters are divided into infinite impulse response (IIR) filter and finite impulse response (FIR) filter. FIR filters don't have the feedback structure i.e, output is connected to the input. It has a strict linear phase characteristic. In this design we need a low pass filter. Low pass FIR filter coefficients are generated from MATLAB software. The two filters in the design are named as FIR1 and FIR2.

FIR filter characteristics are:

a) The phase of FIR filter is strictly linear.

b) The FIR filter is non-recursive structure.

c) Finite precision arithmetic error is very small.

d) Fast Fourier Transformation can be used in FIR filter, while IIR cannot.

e) The order of FIR filter could be large to meet the design specifications.

The bandwidth of the filter is determined by the baseband signal frequency and sampling frequency. It is necessary to specify passband (f_p), stopband (f_s), and transition band when designing a filter. In passband, needed frequencies are passed i.e., needed frequencies are unattenuated. Whereas in stopband, un-needed frequencies stopped i.e., un-needed frequencies are attenuated. Transition band contain frequencies which are lying between the passband and stopband. Therefore, the entire frequency range is split into one or even more passbands, stopbands, and transition bands.

In practical, the magnitude is not necessary to be constant in the passband of a filter. A small amount of ripple is usually allowed in the passband. Similarly, the filter response does not to be zero in the stopband. A small, nonzero value is also tolerable in the stopband. We can see some ripples in the following picture.

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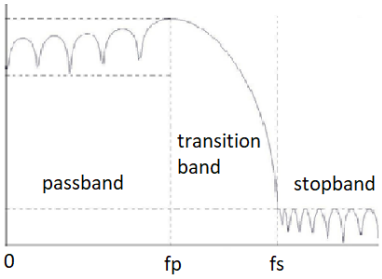

Fig 4. Amplitude-frequency characteristic of lowpass filter

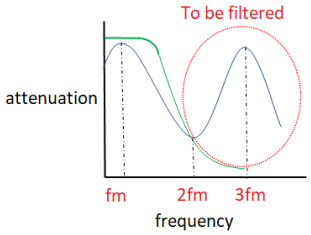

Fig 5. Frequency characteristic of lowpass filter

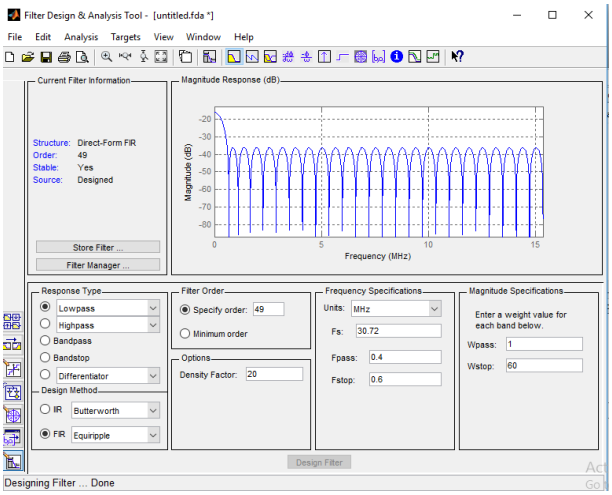

Fig 6. FIR filter 1 design parameters and magnitude response

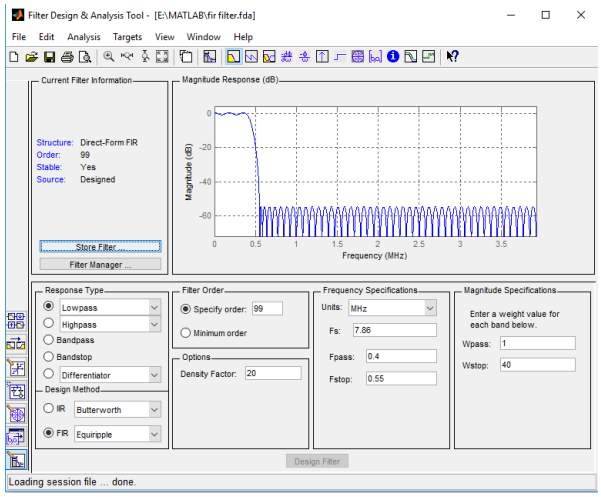

Fig 7. FIR filter 2 design parameters and magnitude response

In this implementation Direct Form FIR filter is used. The message signals x(n), x(n-1), x(n-2),…….x(0) are the message signal samples in digital form i.e, in binary format. The filter coefficients obtained from design of filter in MATLAB are h(n), h(n-1), h(n-2),…….h(0). The intermediate convolution output i.e., delayed message signal samples multiplied with filter coefficients are y(n), y(n-1), y(n-2),…….y(0). The final output of the filter is the sum of all the convolution output which is also known as Sum of Products(SOP).

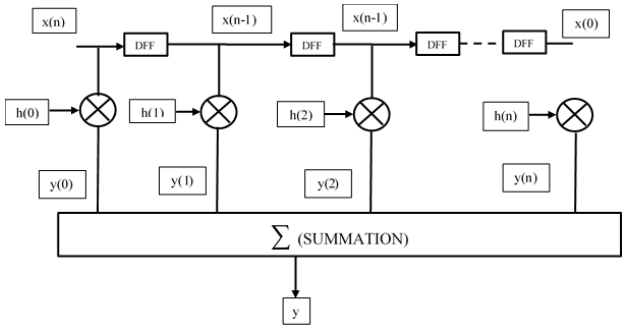

Fig 8. Block diagram of direct form FIR filter

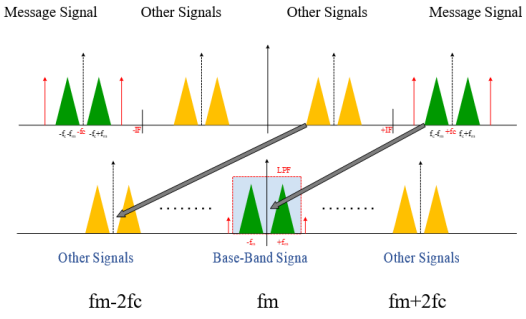

Fig 9. Quadrature Mixing in Frequency Domain

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D. Decimation

Decimation is the process of reducing the sampling rate. The lowpass-filtered signal samples are discarded. Decimation is also known as Down sampling. The decimation factor is the ratio of the input rate to the output rate of the decimator. It is represented as "M". M=input rate / output rate. The calculation and/or memory required to implement a DSP system generally is proportional to the sampling rate, so the use of a lower sampling rate results in low cost. Decimation also reduces the cost of processing. The number of processing operations depends on amount of data (per second) and the length of the filter. If the sampling rate is reduced, the number of operations to implement is also reduced by factor of 2. For the efficient implementation decimation is done in two stages by a factor of 4 and 2. The decimation operation is, considering every M^{th} sample and discarding the $M\text{-}1^{th}$ samples in between. Decimate by 4 means, keep every fourth sample and discard three samples out of every four samples. Since the computations include only one of every M outputs, M-1 operations is reduced per output, an overall "savings" of (M-1)/M. Therefore, the larger the decimation factor is, the larger the savings, percentage-wise. In Verilog the decimation is implemented by the counter logic, where the desired sample is passed to the output after number of cycles equal to the decimation factor.

IV. FINDINGS & ANALYSIS

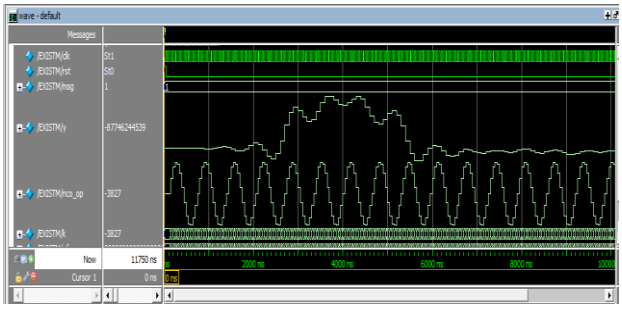

Fig 10. Output of existing model

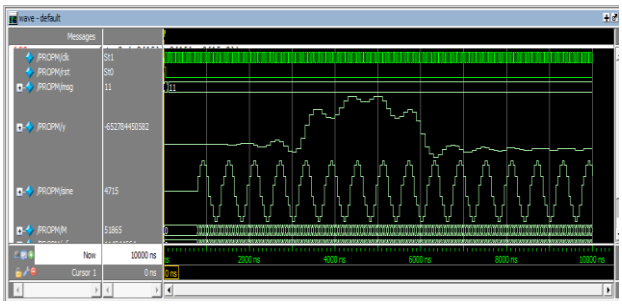

Fig 11. Output of proposed model

V. MATERIALS AND METHOD

- Hardware: Spartan 3e FPGA
- Software: MATLAB R2011b, Simulink, ModelSim SE-6.4

VI. RECOMMENDATIONS

The total dynamic power for implementation of NCO by LUT increases in proportion with number of clock cycles and with increased memory size. LUT based NCO are quite costly in area and power when compared with CORDIC based NCO.

VII. CONCLUSION

Digital Down converters are very essential blocks in any receivers. This paper focuses on the architectural description of the same. Also, it must be noted that the NCO's architecture can be realized either using LUT or CORDIC algorithm. The advantage of LUT over CORDIC is that output latency is just 1, in comparison to CORDIC which has 13 cycles as latency. However, in terms of area, CORDIC consumes lesser area as the RAM requirement for CORDIC is less since no storage of values is involved. However, in terms of RAM requirement, LUT consumes more area as several values of sinusoidal samples have to be seen. Hence, based on this tradeoff, one has to carefully weigh latency vs area parameters before their implementation on hardware.

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