Perspectives in Communication, Embedded-Systems and Signal-Processing (PiCES) – An International Journal
ISSN: 2566-932X, Vol. 4, Issue 6, September 2020
Part of the Proceedings of the 1st All India Paper writing Competition on Emerging Research - PaCER 2020

Low Power High Speed Vedic Techniques in Recent VLSI Design – A Survey

Swathi Dayanand
Student, Department of ECE, BNMIT, Bangalore, India, swathi17ec111@bnmit.in

Varshitha K R
Student, Department of ECE, BNMIT, Bangalore, India, varshitha17ec112@bnmit.in

Rohini T
Assistant Professor, Department of ECE, BNMIT, Bangalore, India, rohinit@bnmit.in

Yasha Jyothi M Shirur
Professor, Department of ECE, BNMIT, Bangalore, India, yashajyothimshirur@bnmit.in

Jyoti R Munavalli
Associate Professor, Department of ECE, BNMIT, Bangalore, India, jyotirmunavalli@bnmit.in

Abstract: Advancement in the Artificial Intelligence (AI) and Machine Learning (ML) has influenced complex designs to be integrated in Very Large-Scale Integration (VLSI) Design. Designers are concentrating on high speed and low power techniques to facilitate the needs of the technology requirements. In multiple AI applications, Digital Signal Processor is the building block, optimization of it may solve the issues related to computation of the data signal at faster rate consuming less power using Vedic mathematics. In this paper, a detailed review is made on recent applications of Vedic Mathematics in the domain of VLSI to yield novel design, efficient architecture for Squarer, Multiplier, Arithmetic unit, Cubic and divider circuits along with their crucial performance criteria. It is deduced that the use of Vedic Sutras in formulating algorithms for digital logic circuit design has led to simplified architecture and yielded higher speed, low power consumption and enhanced efficiency of operation.

Keywords: Vedic mathematics; VLSI; Nikhilam; Urdhva Tiryakbhyam; Yavadunam; Ekanyunena Purvena; Anurupyena

I. INTRODUCTION

The evolution of electronics over time has had a humongous impact on the technological advancements in science and hence provided efficacious methods to improvise and actualize innovations and cutting edge discoveries in many domains, significantly digital signal processing, VLSI ,analog electronics and logic design. As mankind progresses to witness momentous developments in technology it is important to remember that what scientists had envisioned years ago has now turned into a reality not merely on the footing of modern science and mathematics . It is extremely important to recall the precursors of modern science that have manifested richly in ancient Indian scriptures and manuscripts and one of the many striking revelations from the holy Vedas is the ancient system of calculation called Vedic Mathematics.

A. History of Vedic Mathematics

Conceived in the Vedic age, but having remained inconspicuous under centuries of debris, the field Vedic mathematics is a medieval methodology of calculation which has glorified the Indian mathematics since time immemorial, but was only deciphered in the duration 1911-1918 when Sri Bharati Krishna Maharaj, a scholar in the field of Sanskrit, mathematics and philosophy rediscovered the sixteen sutras from the verses of the Atharva Veda. Vedic mathematics has since then gained wide acceptance and has been deemed as the pioneer of modern mathematics.

B. Sutras of Vedic Mathematics

The word 'Vedic' in Vedic mathematics is sourced from the word 'Vedas' that serves as the fountain-head of all knowledge. Vedic Mathematics by the late Bharati Krishna Tirthaji of Govardhana Pitha is a monumental work [50]. In his deep-layer explorations of cryptic Vedic mysteries especially related to the calculus of shorthand formulae and its ample application to practical problems. Bharati Krishna Tirthaji had mastered his unique science and technique, called Yajna, in which other factors like Mantra, Yantra co-operate to yield accuracy and precision for mathematical operations. For this purpose, Tirthaji had developed the six auxiliaries of the Vedas each of which exhibits mathematical skill and adroitness. The Sutras lay down the simplest and elementary guidelines that lays the emphasis for Vedic Mathematics.[49]

Vedic Mathematics is thus a repository of Techniques/Sutras to be able to solve mathematical arithmetic in a quicker and simpler way. It comprises of a set of 16 Sutras and a subset of 13 sub-sutras which can be applied to solve problems in domains of mathematics such as arithmetic, algebra, geometry, and conics. The 16 sutras are mentioned in Table 1.

Name of Vedic Sutra	Meaning of the Vedic Sutra	Use of Vedic Sutra
Ekadhikena Purvena	By one more than the previous one	Useful in finding squares of numbers (like 25x25, 95x95, 105x105, 992x992 etc) and special divisions like 1 divided by 19, 29, 39, …. 199, just in one step.
Nikhilam navatashcaramam dashatah	All from 9 and the last from 10	Useful method for multiplication when numbers are closer to powers of 10 (10,100,1000,…)
Urdhva - tiryakbhyam	Vertically and crosswise	Useful in shortcut multiplication of all kinds of numbers by crosswise multiplication and addition.
Paravartya Yojayet	Transpose and adjust	Useful for division when the divisor is closer to or little greater to the powers of 10.
Shunyam saamyasamuccaye	When the sum is the same that sum is zero	Useful in finding the factors of an equation by equating common terms to zero, also to solve for a variable in a fractional algebraic equation by equating the sum of the Denominators of two fractions having the same numerical numerator to 0.
Anurupye shunyamanyat	If one is in ratio, the other is zero	Useful in solving simple simultaneous equations in which one of the unknown terms are in same proportion to each other as the independent terms are in proportion to each other.
Sankalana vyavakalanabhyam	By addition and by subtraction	Useful to solve simple simultaneous equations which have the co-efficients of the variables interchanged.
Puranapuranabhyam	By the completion or non-completion	Useful in factorizing and solving cubic, quadratic and bi-quadratic equations.
Chalana-kalanabhyam	Differences and similarities	Useful in finding the roots of a quadratic equation as a result of which every quadratic can be broken down into two binomial factors.
Yaavadunam	Whatever the extent of its deficiency	Useful in finding the square of any number closer to the base of powers of 10.
Vyashtisamanstih	Part and whole	Useful for finding the part-whole ratio i.e.., the amount of a given quantity can be found from an overall mixture.
Shesanyankena charamena	The remainders by the last digit	Useful in expressing a fraction as a decimal, to all its decimal places.
Sopaantya-dvayamantyam	The ultimate and twice the penultimate	Useful in multiplication by zero sandwiching technique.
Ekanyunena purvena	By one less than the previous one	Used to multiply a number with repetitions of 9(999…)
Gunitasamuchyah	The product of sum is equal to the sum of product	Useful in finding unknowns in an equation when product of sum is equal to the sum of products.
Gunakasamuchyah	The factors of the sum are equal to the sum of factors	Useful in finding unknowns in an equation when factor of sum is equivalent to the sum of factor.

Table 1. Meaning and Usage of Vedic Mathematic Sutras

II. MATERIALS AND METHODS

This section presents the various articles that are published on the topic Vedic Maths and VLSI. We present how various VLSI applications use Vedic Maths. For presenting this review paper the databases explored are Google Scholar, Science Direct, IEEE Xplore, Research Gate, Elsevier, Web of Science, Knimbus Digital Library and Academia and Springer as seen in Table 2.

Keywords searched: Vedic Maths, Vedic Maths for VLSI, Vedic Maths applications

Name of database	Results yielded
Google scholar	1640
Science Direct	23
IEEE Xplore	2500
Research Gate	840
Elsevier	434
Web of Science	287
Knimbus Digital Library	208
Academia	1059
Springer	65

Table 2. Search databases and results

III. LITERATURE SURVEY

This section discusses the work done by researchers on the applications of Vedic mathematics in Very Large Scale Integration. The basic building blocks of every VLSI design comprises of Datapath, Control Unit, Interconnects and the Memory Unit. The data path makes use of execution units such as Adder, Multiplier, Divider, Shifter circuits in addition to pipeline registers, multiplexers and decoders. Various multipliers such as the serial-parallel multiplier, array multiplier, booth multiplier, Wallace and Baugh Wooley are widely used in VLSI . In our review we discuss some of the methods by which the operation and performance criteria of such multipliers, arithmetic units and dividers have been optimized and made efficient using the useful sutras of Vedic mathematics.

An empirical study with a main objective to illustrate how a Vedic mathematics technique improves the speed of basic mathematical operations has been carried out by K. Karani [1]. The author's study considers some Vedic mathematics techniques, which includes Urdhva Tiryakbhyam Sutra, Nikhilam sutra, with an extensive insight into how the time taken for computation before and after adopting Vedic sutras has differed in terms of minutes. The sub objective of the author is to find the decreased time difference in terms of minutes before and after adopting Vedic mathematics techniques while solving some basic mathematical operations. A hypothesis has been developed by the author to test its significance using paired t-test. The author finds that about 98% respondents out of 25 members agree that Vedic mathematics improves the calculation speed.

The sutras of Vedic Maths can be beneficial if used for the implementation of squarer, multiplier, arithmetic unit, cubic and divider circuits which find a wide application in many fields.

A. Vedic Maths for Squarer circuit application

The importance of a squaring unit for an array of applications such as signal processing to find the transforms or inverse transforms, for cryptography, for high-performance computer graphics ,ALU circuits, and many more digital image processing applications has been highlighted by authors K Durga Bhavani, N V V N J Sri Lakshmi, M Venkat Sai, A Venkatesh, G D Sai Teja[2], and more so the implementation and design of a improved speed squaring unit for binary numbers making use of Yavadunam sutra and the technique bit reduction has been proposed by them. The authors have cited that Yavadunam Tavadunikrtya Vargancha Yojayet is a suitable sutra for squaring. A superior speed and area efficient Yavadunam Square design has been introduced in this sense for binary numbers.

The Yavadunam sutra has been extended to the system of binary numbers and found to work exactly the same as in the system of decimal numbers. The proposed methodology has been found to improvise the current structure of the squaring unit to achieve improvement in area, speed and power.

Authors Prabha S Kasliwal, BP Patil, DK Gautam[48] have also proposed a design for implementing squaring operation using Vedic mathematics in Verilog HDL and also evaluate its performance. The result was this squaring unit is efficient over conventional multipliers and also that it can save area occupied on chip along with resulting in faster computational speed.

B. Vedic Maths for Multiplier application

The significance of Vedic Maths in the high speed multiplier circuit design its FPGA implementation has been dealt with by authors Sudeep.M.C, Sharath Bimba.M and Mahendra Vucha [3] . The authors have come up with a faster method for multiplication based on Urdhva Tiryagbhyam sutra for all cases of multiplication operands and have used the Kogge Stone Algorithm to realize efficient sum of partial products.

A similar approach and similar results have been cited by authors Meghana V, Sandhya S, Aparna R[4] who have enunciated the fact that Vedic Multipliers compute the partial products simultaneously .They have designed a 8 bit multipliers by making use of the lower-bit multiplier cells, therefore giving the resultant multiplier an enhanced as well as modular structure, eventually reducing the complexity of the design.

By the same token we can consider the claim of authors H. Tiwari, G. Gankhuyag, C. Kim, and Y. Cho[28] in their research proving that The algorithms based on conventional mathematics can be simplified and even optimized by the use of Vedic Sutras and a multiplier for low power and high speed applications has been proposed by them.

A multiplier design based on Ekayunena sutra of Vedic Maths has been proposed by authors Khan A, Das R[31]in their design approach of a multiplier. The lesser complexity coupled with simplicity, ease of operation and time saving is a crucial advantage of their design.

We can consider that recently the multipliers based on the Booth's algorithm have become extensively popular in modern VLSI design but we cannot ignore the fact that they come across along with a set of demerits which cannot be neglected. In the Booth's algorithm, the multiplication procedure involves many tedious operations before providing the final product .These tedious operations include/comprise of many comparisons, along with repeated additions and subtractions which eventually reduce the speed of the multiplier in an exponential manner. Given that speed is a critical performance characteristic, employing such a type of multiplier architecture does not serve as a feasible approach owing to the several time consuming operations involved. In order to surpass these disadvantages with regard to speed in the above cited disadvantages, we can explore a new approach

to multiplier design based on ancient Vedic Mathematics.[5]

A design of a trivial high speed multiplier based on Vedic mathematics has been discussed by authors Kahar D, Mehta H [6] and where the authors have emphasized the usefulness of Vedic Maths Sutras for effective decimal number multiplications. The authors mention that the computation process can be speeded up and the time involved in processing can be decreased owing to reduction in combinational path delay.

The work of authors Uttara Bhatt, Deepak Bhoir and K Narayanan has been insightful in presenting the algorithm for a superior speed multiplier which offers reduced propagation delay, as well as optimizes the speed . The design algorithm proposed by authors is based on the Urdhva Tiryakbhyam Vedic sutra.[32]

In continuation to this, we can consider another design of a high speed Vedic multiplier and its implementation that has been discussed by authors Murugesan G and Lavanya S [7] who have utilized the Urdhva-Tiryakbhyam sutra and have proposed an algorithm for multiplying 16 bit value using the designed Vedic Multiplier.

In the same context of speed improvisation benefit of Vedic Maths we can consider the work of authors Deshpande N and Mahajan R[30] who reinstate the claim that Urdhva-Tiryakbhyam sutra has sufficiently improvised the operating speed of existing multiplier circuits. After the implementation of the design using Vedic sutra, it has been observed that the resulting multiplication is efficacious in terms of operating speed.

Along similar lines, authors Panda S, Das R, Sahoo T [24] have worked on an 8-bit multiplier, again, making use of the Vedic sutra called Urdhva-Tiryagbhyam which has been utilized for generation of the partial products, and at the same time improvising the speed of operation.

For realizing improved speed of operation, authors Saha P, Banerjee A, Bhattacharyya P[8] as well as authors M.Nagaraju, R.Surya Prakash, B.Vijay Bhaskar [9] have put forward ASIC design of high speed multiplier for complex numbers using Vedic Maths sutras. The design of this Complex multiplier has been done using multipliers and subtractors based on Vedic sutras. Multiplication of complex is carried out using four multiplications on real parts followed by two additions and subtractions, since most of the existing algorithms for complex number multiplication calls for huge overhead for pre-processing and post-processing otherwise a demand for long latency. It has been substantiated that the Urdhva Tiryakbhyam sutra is best suited for this application.

The novel architecture for the design of a multiplier based on the approach of ROM using Vedic Mathematics has discussed by authors Sriraman L, Prabakar T [27]. The architecture of such a multiplier bears a similarity to that of a Constant Co-efficient Multiplier (KCM) and makes use of Urdhva Tiryakbhyam sutra for multiplication. The resultant is that the obtained multiplier is having 1.5 times superior speed compared to the other multipliers in case of a 16×16 multiplier and it requires only about 76% of the area as that of a 8×8 multiplier and requires only 42% area in case of a 16×16 multiplier.

a) The idea of using compressors in Multipliers

Carrying forward the thoughts of authors Kahar D, Mehta H[6] an improvisation to the existing Vedic Maths multiplier, a novel high speed Vedic Maths multiplier using compressors has been presented by Huddar S, Rupanagudi S, and Kalpana M[10]. A new high speed approach has been proposed by utilizing 4:2 and 7:2 compressors for performing the addition of partial products has been used. A comparison shows that the multiplier design using compressors discussed in their paper, is nearly two times fast as compared to the conventional multiplier. In their work, the authors have applied the same Urdhva Tiryakbhyam sutra to the binary number system in order to make the proposed algorithm easily compatible with the digital hardware. The Multiplier based on this sutra has the benefit because, as the number of bits increases, the gate delay and area increase rather slowly in comparison to other conventional multipliers.

The idea about high speed Vedic multiplier using compressors had also been propounded by authors Pawale P, Ghodke V[11]. They have quoted that for high speed applications, compressors can be used in the architecture of the multiplier to perform the partial product addition.

From the work of authors Harish Kumar and Hemanth Kumar[25], we can decipher that the use of compressors namely the 3:2 compressor, 7:2 compressor and the 4:2 compressor architectures in order to construct an Vedic 8-bit multiplier to help in reducing the gate count as well as provide higher speed.

b) Adders in the multiplier architecture

Authors Pradhan M, Panda R[12] have mooted the idea of a more versatile approach to implement the high speed Vedic multiplier using not only the Nikhilam sutra to reduce the computation time but also the presence of a carry save adder in the architecture of a multiplier will lead to an increase in the computation speed of partial products addition.

Similarly, authors Rajalakshmi T, U Pramila, P Prithra, Mahalakshmi M [13] have proffered the concept of designing a Vedic multiplier using carry select adder. Their work focuses on overcoming the disadvantage of using digital adder in multiplier architecture which results in carry propagation. Carry select adder is widely renowned as one of the fastest among the adder structures. But in this case, a Vedic multiplier is realized in place of conventional multipliers such as the add and shift multiplier, array multiplier[12]. Their design of a 16-bit multiplier which is proposed using the Urdhva Tiryagbhyam sutra has been realized using an 8bit multiplier which in turn done by using a 4-bit multiplier and so forth.

c) Multipliers for high speed low power applications using Vedic Maths : A comparative analysis

In order to cater to applications that require high speed computation such as image processing, digital signal processing, graphics, robotics the basic multiplier architecture will not suffice. These applications require matrix operations, especially matrix multiplication. It is extremely important to have a floating-point multiplier for matrix element multiplication that is not only having superior efficiency but also capable of being configured during run-time, and this has been proposed by authors S. Arish and R. K. Sharma[14]. A customized floating-point format has been used to implement such a run-time reconfigurable multiplier. The authors have used the combination of Karatsuba algorithm and Urdhva Tiryagbhyam sutra which are highly efficient together in order to implement the binary multiplier. A special feature of this design is the effective adjustment of the requisites in terms of delay and power in accordance with varying requirements in accuracy during run time reconfiguration.

Most often, the addition and multiplication operations oversee the execution time despite being the most commonly used binary mathematics operations. in an era of fast, compact, lightweight handheld gadgets, the main aim of any design would be to enhance the speed of multipliers before designing a circuit.[33-35]

Drawing on the shortcomings highlighted by [33-35],the authors A Deepa and C N Marimuthu[15] have exploited the fact that Yavadunam Vedic sutra has not been implemented on any hardware or architecture currently and have thus by extensive research proposed an architecture for a high speed multiplier based on Yavadunam sutra.

There are some relevant findings of the authors that require keen attention:

a. Urdhva Tiryagbhyam sutra proves to be efficient in case of a multiplier for lower order bits, but if the same sutra is extended to higher order bits, the delay will increase. It is evident that an adjustment in terms of delay also leads to increase in the area.

b. Nikhilam Navatash-caramam Dashatah sutra based Vedic multiplier is not very efficient for practical applications owing to its limited input range.

Hence, the authors justify that the proposed Yavadunam multiplier is a better and more reliable.

A similar comparative analysis has been done by authors Mistri N, Somani S and Shete V [29]as they have adduced the comparison of Urdhva Tiryakbhyam and Nikhilam sutra algorithms in order to constructively compare the propagation delay and concluded that the Urdhva Tiryakbhyam sutra offers faster performance for less bit input while Nikhilam sutra offers faster performance for larger inputs.

Amongst all the conventional multipliers like Array, Shift and Add, Braun, Dadda, Wallace and the Urdhva and Nikhilam multipliers, it is proven that the discussed Yavadunam multiplier is clearly having more efficiency in terms of delay for the operands sized greater than 4 bit [15].

The authors A Deepa and C N Marimuthu[15] state that the delay of the proposed Yavadunam multiplier is improved by 49% compared to the Array multiplier, and 27.9% better compared to Braun multiplier, as well as 60.35% better than Shift and Add multiplier, 17.75% superior than Wallace multiplier, 8.81% better than Dadda multiplier, 2.78% better than Urdhva multiplier and 44.46% better than the Nikhilam multiplier. They also reveal that chip-area of the discussed Yavadunam multiplier is 15.43% better compared to Array multiplier, 15.43% improvised than Braun multiplier, 78.45% superior than Shift and Add multiplier, 16.38% preferably better than Wallace multiplier, 5.04% superior than Dadda multiplier, 22.11% superior than Urdhva multiplier and 12.11% better than Nikhilam multiplier. It is also discerned from the same authors that power saving capacity of the proposed Yavadunam multiplier is 92.78% better than Array multiplier, 92.50% better than Braun multiplier, 93.784% superior than Shift and Add multiplier, 89.73% improved than Wallace multiplier, 90.07% better than Dadda multiplier, 87.23% superior than Urdhva multiplier and 29.59% better than Nikhilam multiplier.

In accompaniment to these results authors H. Tiwari, G. Gankhuyag, C. Kim, and Y. Cho have also stated that Vedic multiplier and square are fast in operation than array multiplier and Booth multiplier.[28]

In a measure to realise a higher speed low power as well as area efficient multiplier, the authors Kareem A, Kumar P [16] have proposed the design modified Vedic Maths method. In their paper, Urdhva Tiryagbhyam sutra is applied to the two bit multiplier and the formula is slightly modified and applied for the multiplication of higher order bits.

In the same sense we can consider the work of Patil S, Manjunatha D, and Kiran D[17] which focuses on the development and design of high speed, low power multiplier employing Vedic mathematic techniques. The mentioned multiplier architecture makes use of the Urdhva and Nikhilam sutras of the Vedic Mathematics.

An improvisation in terms of reduced usage of components along with existing providing reduction in critical path delay and increased speed in the yavadunam multiplier has again been discussed by authors Deepa A, Marimuthu C [15].The authors have used the Yavadunam sutra and bit reduction technique to reduce the deficiency bit size to N-1 bits Therefore an N*N bit multiplier is replaced by N-1*N-1.

d) Realisation of efficient digital multipliers

Moving a step ahead towards realisation of efficient digital multipliers for VLSI applications, the authors Deodhe Y, Kakde S, and Deshmukh R [18] have presented a more methodical approach and design methodology for

the improved performance of a digital multiplier based on Vedic Maths sutras and hence, a CMOS multiplier, with lowered amount power consumption and higher linearity is discussed. The critical point is the extent of efficient usage of Vedic sutras in order to achieve a considerable reduction in the number of computational steps as compared to the conventional methods.

A similar implementation of a 16x16 digital multiplier architecture has been observed by the work of R.K. Bathija, R.S. Meena, S. Sarkar and Rajesh Sahu[19] who have proposed a simple 16 bit digital multiplier based on Urdhva Tiryakbhyam Vedic sutra . Two 16 bit binary operands have been considered for multiplication. The important advantage of this method is the observable reduction in power dissipation of this circuit thus giving a minimal value of 0.17 mW and the propagation delay of this multiplier is 27.15ns. These results show an improvement in power dissipations and delays seen in Booth, Array, Wallace Tree multipliers.

The ample proof and justification of the efficiency of Urdhva Tiryakbhyam sutra in optimising the multiplier architecture has been provided in the work of Ganesh Kumar G, Charishma V[20] who have illustrated the Verilog HDL simulation results of Urdhva Tiryakbhyam Sutra for 32x32 bits multiplier and its FPGA implementation using Xilinx Synthesis Tool on Spartan 3E kit. The results obtained upon synthesis show that the computation time is merely 31.526 nanoseconds.

Likewise, authors Koushighan S, Hariharan K, Vaithiyanathan V[21] are having similar findings in the performance results of Vedic multipliers as opposed to conventional ones and they accentuate that Vedic mathematics gives prospective solutions for easily obtaining the results. Their design and simulation has been carried out using Verilog HDL and ModelSim ALTERA 6.5b and Xilinx ISE Design Suite 13.2.

C. Vedic Maths for Artithmetic unit application

The significance of an arithmetic unit in electronics is well known. An arithmetic unit (AU) is widely used popularly for image and signal processing applications. These AU's implement multiple functionalities and comprise of multiplier as their critical element.

The very consequence of a high speed and area efficient arithmetic unit using Vedic mathematics has been brought to the light by authors K.N. Vijeyakumar, S.Kalaiselvi, K.Saranya [22].They have recommended the use of Urdhva Tiryakbhyam sutra for the multiplier design to yield a low generation unit in multiplier which offers low complexity for partial product generation and helps in significantly reducing the critical delay. The authors[22] cite that the digital implementation of the proposed arithmetic unit has resulted in delay reduction of 13.7% and area-delay-product(ADP) reduction of 19.2% along with the area reduction of 17.9% and moreover the Urdhva Tiryakbhyam based arithmetic unit realizes superior ADP saving, with the ADP of their own proposed design reducing by 35.6% and 19.2% in comparison to "MORA - An Architecture and Programming Model for a Resource Efficient Coarse Grained Reconfigurable Processor".

Similarly authors Ramalatha M ,Deena Dayalan, K Dharani P [26] have exemplified that the multiplier block of an ALU can be realized efficiently using the Urdhva Tiryagbhyam-Vedic sutra for realizing a multiplier that contributes to a striking difference in the original process of multiplication itself because it enables the generation of intermediate products parallelly, thus eliminating unwanted multiplication steps. To add to this, the use of the Karatsuba algorithm provides the much needed compatibility to different data types.

D. Vedic Maths for Cubic circuit implementation

Anurupyena Sutra of Vedic Mathematics states that "If you start with the cube of the first digit and take the next three numbers(in the top row) in a Geometrical Proportion (in the ratio of the original digits themselves) you will find that the 4th figure (on the right end) is just the cube of the second digit".[43]

The insightful concept of an algorithm for cubic computation using Vedic mathematics ban been bright to the fore by authors Kumar D, Saha P, Dandapat A [23] who opine that the an algorithm for cubic operation using 'Vedic mathematics' formulae can noticeably lessen some of the important VLSI design aspects such as propagation delay as well as the dynamic power consumption in watts as also agreed upon by authors Vaijyanath K, Linganagouda K and Subhash K[35]. In this regard these authors discuss the prospects of Anurupyena sutra and Yavadunam sutra for efficient realisation of a cubic algorithm. In the proposed 8 bit cubic circuitry, the values for propagation delay and the relative power consumed by the reported 8-bit cubic circuit upon introspection was found to be ~5.5 ns and ~2.6 mW respectively. Propagation delay was found to have been enhanced by ~12% and power consumed was decreased by ~22% as compared to the conventional cubic architecture.

Authors V. Kunchigi, L. Kulkarni, S. Kulkarni[42] have proposed the design for low power cubing architecture using the Urdhva Tiryagbhyam sutra and Anurupyena sutra Vedic sutras and opines that the Anurupyena sutra of Vedic mathematics offers an efficient alternative for the construction of a cubing circuit excluding the use of the conventional methods of multiplication. The discussed architecture helps in lowering of the total power consumed by 45% and also the area by 63% in comparison to the conventional architecture.

Authors H. Thapliyal, S. Kotiyal, M.B. Srinivas [43] also have proposed a cubic circuit architecture utilising the principles of Anurupyena sutra and have demonstrated a noticeable improvement in area and delay reduction using histograms for comparison with conventional architecture.

E. Vedic Maths for Divider application

A Divider circuit can be designed to suit the need of an application. The authors Prabir Saha, Arindam Banerjee, P Bhattacharyya[37] and A Dandapat have illustrated division Using Nikhilam Navatas-caramam Dasatah sutra. Similarly, 16-bit by 8-bit division circuit architecture based on one of the sutra of ancient Vedic Maths is proposed by author Soma BhanuTej [38].

Another novel Division is carried out using the Dhwajanka (dhwajam) sutra of Vedic Maths by R.Thamil Chelvani, S.Roobini Priya[39].

Authors Ratiranjan Senapat, Bandan Kumar Bhoi, Manoranjan [40] have proposed the design of a Vedic divider using Xilinx ISE on 90nm CMOS technology using the Paravartya Yojayet sutra. They have implemented an 8 bit by 4 bit divider circuit and their findings are that the propagation delay was a minimum time of ~19.9ns and power consumed that is ~34mW is also meagre . Hence, the authors cite that when compared to division using repetitive subtraction method their algorithm had ~46% less propagation delay and consumption of power was reduced by ~27% .The design of a low power consuming 16 Bit Vedic divider for the purpose of superior speed VLSI design has been proposed by authors Kuldeep Singh Sidhu and Ashwani Kumar Singla[24], an algorithm based on the sutra "Paravartya Yojayet" is applied for realizing the reduction in the power consumed as well as provide high speed. The proposed Vedic divider circuit has been used to carry out 8-bit by 4 bit division where the total power dissipation is 12.75mw and it produces total propagation delay nearly to 5.83ns. The comparison result shows that proposed division method provides 70% less delay, 62% reduction in total power and 88% less PDP(power delay product) as compared to a novel binary divider, as well as 16 bit by 8 bit division where the simulation results shows that Vedic divider using 13 transistor full adder provides 13% delay reduction, 7% reduction in total power dissipation and 20% less PDP against 26transistor full adder.

Similarly, authors Shivani Madhok, Kavita Goswami, Tanesh Kumar[47] have put forth an energy efficient Vedic Divider using the "Paravartya Yojayet" sutra called Energy Efficient Vedic Divider using Paravartya Yojayet on 28nm FGPA based on Capacitance Scaling .

In continuation to previous findings, authors Shantanu Oke, Suraj Lulla, and Prathamesh have suggested the usage of Dhwajam Vedic Maths sutra to design Distinctive Division Architecture for a divider circuit and they have implemented their algorithms on Xilinx 8.1 ISE along with testing the obtained results on Spartan 3 FPGA platform . The authors have also compared their algorithm with one of the prominent existing algorithms/techniques for division such as Newton- Raphson algorithm, and the authors have found that their algorithm was simple in terms of complexity and used less number of steps(iterations) and there was no need for any look up table in their proposed algorithm as was the requirement in case of Newton-Raphson and SRT algorithm.

F. Discussion and Future Scope

With regard to the observations and inferences mentioned above we discern that for a multiplier circuit amongst the various architectures that have been proposed for methodical and coherent operation using appropriate sutras of Vedic mathematics it is unarguably the multiplier architecture using The Yavadunam sutra yields the most optimum design parameters including delay, area and power consumption.

However, for the case of digital multiplier circuits, we find that the Urdhva Tiryakbhyam sutra is more suitable to cater to needs such as low dissipation of power and delay.

Additionally since some of the multipliers deploy an adder in their architecture, it was found that, switching activity an adder influences the power consumed and in order for us to overcome this drawback authors Jan M. Rabaey and Massoud Pedram [44] say that the considered fixed bit operand could be changed or increased in the encoding scheme and hence reduction in power can be realized by improvising the ratio of partial product compression for the upcoming designs in the near future for low power VLSI design, also we have seen the Urdhva Tiryakbhyam sutra has been used for partial product generation can be further studied to lead towards superior partial product compression.

Talking about the squarer circuit authors P. S. Kasliwal, B. P. Patil, and D. K. Gautam [48] assert that the Urdhva Tiryakbhyam sutra comparably provides a faster algorithm for squaring, which when implemented on an FPGA will yield a good technique for speeding up the DSP and Encryption. They mention that their squaring unit is efficient in comparison to conventional squaring circuits and that it can save area occupied on chip and along with providing faster computational speed. This will eventually save hardware cost and operating cost as well, thus making it an attractive option beside the other ones.

As for the arithmetic unit architecture that has been discussed by most authors suggests that the Urdhva Tiryakbhyam sutra is best suited for this purpose as it is proven to ascertain the claims of area, area-delay-product (ADP) reduction in the arithmetic unit.

The future scope in the design of arithmetic unit could be working towards implementation of AU for improvised double precision, coupled with power saving techniques in current architecture using block isolation. As for the double precision (floating-point) format, it is a computer number format, that usually occupies 64-bits in the computer memory and hence represents a broad range of dynamic numerals by making use of a floating radix point. In order to design an AU for double precision, the floating point unit that has to be implemented consists of the four sub units namely adder, subtractor, multiplier and divider

says author B Chittaluri [45] and there is scope for further research to improvise the architecture of these blocks using appropriate Vedic Maths sutras.

Coming to the cubic circuit architecture implementation, we mention, and many authors cite that the Anurupyena sutra is indisputably best suited for cubic operation owing to its inherent property of simplifying the cubing procedure. Owing to some of the factors such as, speed, low power consumption, timing efficiency and less area the proposed Vedic square and cube can be implemented in Arithmetic and Logical Units and serve as a replacement for the traditional square and cube circuits says author P Ramanamma [46] and the very idea proposed by the author might pave the way for future research in this direction that would be to research for reducing area requirements.

Lastly, upon introspecting the work done to realize an efficient divider circuit we infer from the findings of referred authors that the Paravartya Yojayet Vedic sutra is advantageous because of reduction in power consumed, delay as well as power-delay-product(PDP) and such a divider architecture conforms to the desired requirements of speed. Authors S. Madhok, K. Goswami, and T. Kumar [47] who had proposed a design for, "Capacitance Scaling Based Energy Efficient Vedic Divider using Paravartya Yojayet on 28nm FGPA," mention that the futuristic scope for their Vedic divider based on capacitance scaling and relying on Paravartya Yojayet lies in implementing the same design on 22nm or 18 nm FGPA. The authors also suggest that the Vedic divider can be re-designed with alternative techniques such frequency scaling, thermal scaling, clock gating, along with impedance matching with different logic families which also offer energy efficiency.

IV. CONCLUSION

From the observed practical designs and implementations, we find that Vedic mathematics essays an instrumental role in simplifying as well as rationalizing most of the tedious and cumbersome mathematical operations. The Vedic sutras serve as an archive of ancient knowledge and as a luminary of important mathematical foundations . Vedic mathematics has profound scope for application in various domains of Engineering and Technology. This engrossing field presents an array of effectual applications in the design of elementary VLSI circuits albeit the fact that there are specific sutras to cater to particular operations. The field of Vedic Maths is potent in aspects of significantly alleviating the commonly encountered problems in VLSI design such as timing delay, power consumption, chip area among others. Moreover, as the fabrication industry is seeing manifold development there is a dearth for design of algorithms which are fast and efficient and such algorithms can be devised using Vedic sutras to meet the required needs. Also, as the VLSI design industry is progressing towards automation of layout process, since the fabrication cost is a rapid growing function of circuit area there is ample scope for devising algorithms for to optimize the layout area along with delay minimization. There is abundant scope for research focusing on enhancing existing algorithms and design architectures to obtain improved results.

ACKNOWLEDGEMENTS

We whole heartedly thank BNMIT Management and Visvesvaraya Technological University Belgaum for encouraging us to carry out the research in this area and publish the paper in a reputed journal.

REFERENCES

[1] K. P. Karani, "An empirical study on role of Vedic mathematics in improving the speed of basic mathematical operations", "ISSN : 2249-0558," no. April, 2017.

[2] K Durga Bhavani, N V N J Sri Lakshmi, M Venkat Sai, A Venkatesh, G D Sai Teja, "High speed VLSI Squaring unit of Binary Number Design with Yavadunam Sutra and Bit Reduction, Int. J. Innov. Technol. Explor. Eng., vol. 9, no. 2, pp . 775–778, 2019, doi: 10.35940/ijitee.b6879.129219.

[3] S. M.C, S. Bimba.M, and M. Vucha, "Design and FPGA Implementation of High Speed Vedic Multiplier," Int. J. Comput. Appl., vol. 90, no. 16, pp. 6–9, 2014, doi: 10.5120/15802-4641.

[4] V. Meghana, S. Sandhya, R. Aparna, and C. Gururaj, "High speed multiplier implementation based on Vedic Mathematics," in 2015 International Conference on Smart Sensors and Systems, IC-SSS 2015, 2017, doi: 10.1109/SMARTSENS.2015.7873593.

[5] G. Sameer, M. Sumana and S. Kumar, "Novel High Speed Vedic Mathematics Multiplier using Compressors" International Journal of Advanced Technology and Innovative Research, Vol.7, Issue.2, pp.0244-0248, 2015.

[6] D. K. Kahar and H. Mehta, "High speed Vedic multiplier used Vedic mathematics," in Proceedings of the 2017 International Conference on Intelligent Computing and Control Systems, ICICCS 2017, 2017, vol. 2018-Janua, pp. 356–359, doi: 10.1109/ICCONS.2017.8250742.

[7] G. Murugesan and S. Lavanya, "Design and implementation of high speed multiplier using Vedic mathematics," ARPN J. Eng. Appl. Sci., vol. 10, no. 16, pp. 6758–6764, 2015.

[8] P. Saha, A. Banerjee, P. Bhattacharyya, and A. Dandapat, "High speed ASIC design of complex multiplier using Vedic mathematics," TechSym 2011- Proc. 2011 IEEE Students' Technol. Symp., vol. 3, no. 1, pp. 237–241, 2011, doi: 10.1109/TECHSYM.2011.5783852.

[9] Nagaraju, M., R. Surya Prakash and Bolguddu Vijay Bhaskar. "High Speed ASIC Design of Complex Multiplier Using Vedic Mathematics." (2013).

[10] S. R. Huddar, S. R. Rupanagudi, M. Kalpana, and S. Mohan, "Novel high speed Vedic mathematics multiplier using compressors," in Proceedings - 2013 IEEE International Multi Conference on Automation, Computing, Control, Communication and Compressed Sensing, iMac4s 2013, 2013, pp. 465–469, doi: 10.1109/iMac4s.2013.6526456.

[11] P. D. Pawale and V. N. Ghodke, "High speed Vedic multiplier design and implementation on FPGA," Int. J. Appl. Res., vol. 1, no. 7, pp. 239–244, 2015.

[12] M. Pradhan and R. Panda, "High speed multiplier using Nikhilam Sutra algorithm of Vedic mathematics," Int. J. Electron., vol. 101, no. 3, pp. 300–307, 2014, doi: 10.1080/00207217.2013.780298.

[13] T. Rajalakshmi and M. R. Mahalakshmi, "Design of Vedic Multiplier Using SQRT Carry Select Adder (CSLA) ," Int. J. MC

Sq. Sci. Res., vol. 9, no. 1, pp. 34–43, 2017, doi: 10.20894/ijmsr.117.009.001.005.

[14] S. Arish and R. K. Sharma, "Run-Time-Reconfigurable Multi-Precision Floating-Point Matrix Multiplier Intellectual Property Core on FPGA," Circuits, Syst. Signal Process., vol. 36, no. 3, pp. 998–1026, 2017, doi: 10.1007/s00034-016-0335-2.

[15] A. Deepa and C. N. Marimuthu, "High Speed VLSI Architecture for Squaring Binary Numbers Using Yavadunam Sutra and Bit Reduction Technique," Int. J. Appl. Eng.

[16] V. M. and P. Kumar, "VLSI Implementation of High Speed-Low Power-Area Efficient Multiplier Using Modified Vedic Mathematical Techniques," Recent Patents Comput. Sci., vol. 9, pp. 216–221, Jan. 2017, doi: 10.2174/2213275908666150220203501.

[17] S. Patil, D. Manjunatha, and D. Kiran, Design of speed and power efficient multipliers using Vedic mathematics with VLSI implementation. 2014.

[18] Y. Deodhe, S. Kakde, and R. Deshmukh, Design and Implementation of 8-Bit Vedic Multiplier Using CMOS Logic. 2013.

[19] R. K.Bathija, R. S. Meena, S. Sarkar, and R. Sahu, "Low Power High Speed 16x16 bit Multiplier using Vedic Mathematics," Int. J. Comput. Appl., vol. 59, no. 6, pp. 41–44, 2012, doi: 10.5120/9556-4016.

[20] G. Ganesh Kumar and V. Charishma, "Design of High Speed Vedic Multiplier using Vedic Mathematics Techniques," Int. J. Sci. Res. Publ., vol. 2, no. 1, pp. 2250–3153, 2012, [Online]. Available: www.ijsrp.org.

[21] S. Koushighan, K. Hariharan, and V. Vaithiyanathan, "Design of an optimized high speed multiplier using Vedic mathematics," Contemp. Eng. Sci., vol. 7, no. 9–12, pp. 443–448, 2014, doi: 10.12988/ces.2014.4328.

[22] V. K N, K. S, and S. K, "Vlsi Implementation of High Speed Area Efficient Arithmetic Unit Using Vedic Mathematics," ICTACT J. Microelectron., vol. 2, no. 1, pp. 198–202, 2016, doi: 10.21917/ijme.2016.0034.

[23] D. Kumar, P. Saha, and A. Dandapat, "Vedic algorithm for cubic computation and VLSI implementation," Eng. Sci. Technol. an Int. J., vol. 20, no. 5, pp. 1494–1499, 2017, doi: 10.1016/j.jestch.2017.10.001.

[24] S. Panda, R. Das, S. Raheman, and T. Sahoo, "VLSI Implementation of Vedic Multiplier Using Urdhva– Tiryakbhyam Sutra in VHDL Environment: A Novelty," IOSR J. VLSI SIGNAL Process., vol. Volume 5, p. PP 17-24, Feb. 2015, doi: 10.9790/4200-05131724.

[25] Harish Kumar and Hemanth Kumar A R, "Design and Implementation of Vedic Multiplier using Compressors," Int. J. Eng. Res., vol. V4, no. 06, pp. 230–233, 2015, doi: 10.17577/ijertv4is060321.

[26] R. Marimuthu, K. Dayalan, P. Dharani, and S. Priya, High speed energy efficient ALU design using Vedic multiplication techniques. 2009.

[27] L. Sriraman and T. Prabakar, "Design and implementation of two variable multiplier using KCM and Vedic Mathematics," Mar. 2012, doi: 1109/RAIT.2012.6194554.

[28] H. Tiwari, G. Gankhuyag, C. Kim, and Y. Cho, Multiplier design based on ancient Indian Vedic Mathematics, vol. 2. 2008.

[29] N. R. Mistri, S. B. Somani, and V. V. Shete, "Design and comparison of multiplier using Vedic mathematics," in Proceedings of the International Conference on Inventive Computation Technologies, ICICT 2016, 2016, vol. 2, doi: 10.1109/INVENTIVE.2016.7824870.

[30] N. G. Deshpande and R. Mahajan, "" Ancient Indian Vedic Mathematics Based Multiplier Design for High Speed and Low Power Processor "," in International Journal of Advanced Research in Electrical, 2014, vol. 3, no. 4

[31] A. Khan and R. Das, "Novel approach of multiplier design using ancient Vedic mathematics," in Advances in Intelligent Systems and Computing, 2015, vol. 340, pp. 265–272, doi: 10.1007/978-81-322-2247-7_28.

[32] U. B., "HIGH SPEED MULTIPLIER USING VEDIC MATHEMATICS," Int. J. Res. Eng. Technol., vol. 03, no. 01, pp. 548–552, 2014, doi: 10.15623/ijret.2014.0301092.

[33] Richa S, Manjit K and Gurmohan S 2015 Design and FPGA implementation of optimized 32-bit Vedic multiplier and square architectures In: Proceedings of the international conference on Industrial instrumentation and control.

[34] Sriraman L, Saravana Kumar K and Prabakar T N 2013 Design and FPGA implementation of binarysquarer using Vedic mathematics In: Proceedings of the 4th international conference on computing, communication and networking technologies.

[35] Vaijyanath K, Linganagouda K and Subhash K 2013 Low power square and cube architectures using Vedic Sutras. In: Proceedings of the 5th international conference on signal and image processing.

[36] "Design and simulation of 64 bit divider using Vedic Maths" no. January, 2017, doi: 01.0401/ijaict.2014.07.18.

[37] Prabir Saha, Arindam Banerjee, Partha Bhattacharyya, Anup Dandapat, "Vedic Divider: Novel Architecture (ASIC) For High Speed VLSI Applications", International Symposium On Electronics System Design,pp-67-71,2011.

[38] Soma BhanuTej," Vedic Divider-A High performance Computing Algorithm For VLSI Application", IBM system and Technology Groups''.

[39] R.Thamil Chelvan, S.Roobini Priya," Implementation of Fixed and Floating Point Division Using Dhvajanka Sutra".

[40] Ratiranjan Senapati, Bandan Kumar Bhoi, Manoranjan Pradhan (2013) 'Novel Binary Divider Architecture for high speed VLSI applications', Proceedings of 2013 I.E.E.E. Conference on Information and Communication Technologies.

[41] Shantanu Oke, Suraj Lulla, Prathamesh Lad (2014) 'VLSI (FPGA) Design for Distinctive Division Architecture using the Vedic Sutra 'Dhwajam'', International Conference on Devices, Circuits and Systems(ICDCS)

[42] V. Kunchigi, L. Kulkarni, S. Kulkarni, Low power square and cube architectures using Vedic sutras, in: Proc. of Fifth Int. Conf. on Signal and Image Processing(ICSIP), Jeju Island, 2014, pp. 354–358.

[43] H. Thapliyal, S. Kotiyal, M.B. Srinivas, Design and analysis of A novel parallel square and cube architecture based on ancient Indian Vedic mathematics, in:48th Midwest Symp. on Circuits and Systems, KY, USA, 2005, pp. 1462–1465.

[44] Jan M. Rabaey and Massoud Pedram "LOW POWER DESIGN METHODOLOGIES", Springer Science and Business Media New York,1996.

[45] B. Chittaluri, "Implementation of Area Efficient IEEE-754 Double Precision Floating Point Arithmetic Unit Using Verilog," vol. 2, no. 12, pp. 15–21, 2015.

[46] Ramanamma.P, "low power square and cube architectures using Vedic sutras", International Journal of Engineering Research and General Science Volume 5, Issue 3, May-June, 2017

[47] S. Madhok, K. Goswami, and T. Kumar, "Capacitance Scaling Based Energy Efficient Vedic Divider using Paravartya Yojayet on 28nm FGPA," Gyancity J. Eng. Technol., vol. 2, no. 1, pp. 18–30, 2016, doi: 10.21058/gjet.2016.2103.

[48] P. S. Kasliwal, B. P. Patil, and D. K. Gautam, "Performance evaluation of squaring operation by Vedic mathematics," IETE J. Res., vol. 57, no. 1, pp. 39–41, 2011, doi: 10.4103/0377-2063.78327.

[49] T. A. A. Broadbent and J. Shankaracharya, "Vedic Mathematics," Math. Gaz., vol. 50, no. 374, p. 440, 1966, doi: 10.2307/3613999.

[50] Jagadguru Swami Sri Bharati Krisna Tirthaji Maharaja, Vedic Mathematics: Sixteen Simple Mathematical Formulae from the Veda, Delhi (1965).