Complex Multiplier Architectures on VLSI

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Abstract: Complex number multipliers are the mainstay for Digital Signal Processing (DSP) algorithms and for many other scientific applications. Multipliers are the slowest elements in the system due to their circuit complexity. Hence, they play key role in deciding system's performance. Thus, it is necessary to reduce the complexity of these operations at architectural level and can save the chip area and further speed and power parameters can be optimized. In this paper, literature survey of various papers related to Multipliers are carried out.

Keywords: Multipliers; VLSI; Complex Numbers; FPGA; Booth; Modified Booth

I. INTRODUCTION

The basic arithmetic operations performed in most of the systems are addition, subtraction, multiplication and division. Among these operations, multiplication operation slows the system's performance. The speed of multiplier determines the speed of the processor. The performance of many computational problems is analyzed by the speed at which multiplication operation can be executed. Immense hardware resources are utilized to increase the speed of the multiplier. So, there is a need to design high speed and area efficient multiplier architecture. Based on literature survey of Multiplier and Complex Number Multiplier there exist drawback in optimizing area. This paper focuses on such the survey conducted towards implementation of a multiplier to explore its VLSI perspective.

II. LITERATURE SURVEY

A. Paper Title: Efficient Complex-Number Multipliers Mapped On FPGA

Authors: A. P. Pascual, J. Valls and M.M. Peiro

In this paper, they have used offset binary coded (OBC) with distributed arithmetic (DA) and many of the authors expressed this method as an area efficient method to implement VLSI systems. Distributed arithmetic is used to design complex number multipliers and implemented on FPGA using both DA and OBC-DA techniques. In FPGA based complex multipliers, DA method gives better performance. But OBC technique will not give improvements in FPGA design. Drawback is the algorithm that computes binary offset-binary code is more complex and hence the area occupied is higher and throughput lower.

B. Paper Title: An Efficient Modified Booth Multiplier Architecture

Authors: Razaidi Hussin, Ali Yeon Md. Shakaff, Norina Idris, Zaliman Sauli, Rizalafande Che Ismail and Afzan Kamarudin

In this paper, they propose an efficient Modified Booth Multiplier architecture based on Radix 4 Booth multiplier. To improve this architecture two enhancements were done. First is to modify the Wen-Chang's Modified Booth Encoder (MBE) and second is to improve the delay in 4:2 compressor circuit. The objective of developing the fast multiplier has been achieved with 136.4 ns, 246.8 ns and 467.8 ns for 8-bit, 16-bit and 32-bit multipliers respectively. This is 2% to 7% improvement compared to other designs. The multiplier designed over here has slight disadvantage in size because the faster Booth Encoder (BE) is not the smallest scheme.

C. Paper Title: Design of Area and Power Efficient Complex Number Multiplier

Authors: Premananda B.S, Samarth S. Pai, Shashank B, Shashank S. Bhat

In this paper, high speed 8-bit complex number multiplier is designed using Vedic Mathematics i.e. Urdhva Tiryagbhyam (Vertically and Cross-Wise) sutra and carry skip adder technique. The proposed 8-bit Multiplier results in a 6.23% increase in speed, 1.88% decrease in power dissipation when compared to normal 8-bit Vedic Multiplier. Further, proposed 8-bit Complex Number Multiplier results in 9.11% decrease in power dissipated and 1.75% decrease in area compared to normal 8-bit Complex Number Vedic Multiplier.

D. Paper Title: Review on 32-Bit IEEE 754 Complex Number Multiplier Based on FFT Architecture using BOOTH Algorithm

Authors: Anuja A. Bhat, Prof. Mangesh N. Thakare

In this paper, they have shown review of high speed, less power and less delay 32-bit IEEE 754 Floating Point Complex Multiplier using Booth Algorithm that includes 32-bit Floating Point Adder, Subtractor and Multiplier. The main objective of this research is to reduce delay, power and to increase the speed.

E. Paper Title: Implementation of Baugh-Wooley Multiplier and Modified Baugh Wooley Multiplier Using Cadence (Encounter) RTL

Authors: Pramod S. Aswale, Mukesh P. Mahajan, Manjul V. Nikumbh, Omkar S. Vaidya

This paper presents an efficient implementation of a high speed, low power multiplier using shift and adds methods of Baugh Wooley Multiplier. This study presented the design and implementation of Baugh Wooley multipliers using Cadence (Encounter) RTL Complier. In this work, Modified Baugh Wooley is having least area, power and delay. The Modified Baugh Wooley architecture is 109X faster than Conventional array multiplier and 102X faster than conventional Baugh Wooley. The operating frequency of 5 x 5 Design Modified Baugh Wooley multiplier is 160MHz. The Selection of Multiplier should be done depending on performance measure and application nature. Baugh Wooley consumes more power as compared to conventional Baugh Wooley.

F. Paper Title: FPGA Implementation of high speed 8-bit Vedic multiplier using barrel shifter.

Authors: Pavan Kumar U.C.S, Saiprasad Goud A, A.Radhika

In this paper, 8-bit Vedic Multiplier is improved in terms of propagation delay when compared with conventional multipliers like array multiplier, Brawn multiplier, modified booth multiplier, Wallace tree multiplier. In the proposed design, 8-bit barrel shifter is used which requires only one clock cycle for 'n' number of shifts. The propagation delay comparison was extracted from synthesis report and static timing report. Finally, delay was reduced with 45% when compared to array multiplier, booth multiplier and conventional vedic multiplier on FPGA. These high-speed multipliers are used in image processing, arithmetic logic unit and VLSI signal processing.

G. Paper Title: FPGA Implementation of Complex Multiplier Using Minimum Delay Vedic Real Multiplier Architecture.

Authors: K. Deergha Rao, Ch. Gangadhar, Praveen K Korrai

This paper presents the design of Vedic real multipliers based on Urdhva sutra. Here, four real multiplier solution and three real multiplier solution are presented for Vedic complex multiplier. The two solutions of complex multiplier are implemented using VHDL. Parameters like path delay, logic power, power, number of slices LUT's, number of bonded IOB's are compared with all other multipliers. It is observed that Vedic complex multiplier is more efficient taking less path delay and less power consumption compared to Booth complex multiplier but consumes more power than the array complex multiplier. Further, Vedic complex multiplier implemented by four real multiplier solution is faster than three real multiplier solution with increase in power consumption.

H. Paper Title: A Well-Structured Modified Booth Multiplier Design

Authors: Li-Rong Wang, Shyh-Jye Jou and Chung-Len Lee

Description: In this paper, well-structured MBE multiplier design has been presented. The design is well-structured because an improved modified Booth encoder and selector is devised so that rearranging and reducing partial products to achieve an extra-row-removal for the multiplier is possible. Also, a hybrid spare-tree structure is used in designing two's complementation circuit. This method reduces the area and improve the speed. According to the experimental results, the design can obtain 15.8% and 11.7% on the area and power savings respectively over the classical design and 7.5% and 5.5% area and power saving respectively over the design which was reported to give the best performance.

I. Paper Title: Design of Speed and Power Efficient Multipliers Using Vedic Mathematics with VLSI Implementation

Authors: Savita Patil, D. V. Manjunatha, Divya Kiran

Multiplier is most important hardware block for many applications such as image processing, signal processing. In these applications, high speed multiplication with low power consumption is required. In this paper two multipliers are designed. One using Urdhva sutra and the using Nikhilam sutra from Vedic Mathematics. These multipliers are developed using an ASIC methodology in 65 nm technology. Urdhva and Nikhilam multipliers implemented using modified full adder are 60% and 77% faster and consumes 37% and 50% less power than that of array multiplier.

III. CONCLUSION

As per the literature survey it is observed that many different approaches that has implemented to design multipliers are resource expensive. None of the existing papers include Complex Number Multipliers designed using Nikhilam sutra. In many papers the methods adopted to design multipliers have not optimized in terms area. In few papers, drawback lies in power optimization. Thus, we are going to design a Complex Number Multiplier using Nikhilam sutra. The main focus of the work is to implement an area efficient system with less resource utility. In this paper, results of various multipliers such as Booth multiplier, Modified Booth Multiplier and Urdhva Multiplier are compared with Vedic Complex Number Multiplier designed using Nikhilam sutra. We will prove that our proposed architecture is less resource expensive and area efficient.

REFERENCES

[1] A. P. Pascual, J. Valls and M. M. Peiro, "Efficient complex-number multipliers mapped on FPGA," ICECS'99. Proceedings of ICECS '99. 6th IEEE International Conference on Electronics, Circuits and Systems (Cat. No.99EX357), Pafos, Cyprus, 1999, pp. 1123-1126 vol.2.

[2] R. Hussin, A. Y. M. Shakaff, N. Idris, Z. Sauli, R. C. Ismail and A. Kamarudin, "An efficient Modified Booth multiplier architecture," 2008 International Conference on Electronic Design, Penang, 2008, pp. 1-4, doi: 10.1109/ICED.2008.4786767.

[3] B. S. Premananda, S. S. Pai, B. Shashank and S. S. Bhat, "Design of area and power efficient complex number multiplier," Fifth International Conference on Computing, Communications and

Networking Technologies (ICCCNT), Hefei, 2014, pp. 1-5, doi: 10.1109/ICCCNT.2014.6963017.

[4] N.Thakare, A.A. (2017). Review on 32-Bit IEEE 754 Complex Number Multiplier Based on FFT Architecture using BOOTH Algorithm. International Journal of Engineering and Computer Science, 6.

[5] Mahajan, Mukesh & aswale, Pramod & vaidya, Omkar & nikumbh, Manjul. (2015). Implementation of Baugh-Wooely Multiplier and Modified Baugh Wooely Multiplier Using Cadence (Encounter) RTL. IJSETR. 4. 293-298.

[6] U. C. S. Pavan Kumar, A. Saiprasad Goud and A. Radhika, "FPGA implementation of high speed 8-bit Vedic multiplier using barrel shifter," 2013 International Conference on Energy Efficient Technologies for Sustainability, Nagercoil, 2013, pp. 14-17, doi: 10.1109/ICEETS.2013.6533349.

[7] K. D. Rao, C. Gangadhar and P. K. Korrai, "FPGA implementation of complex multiplier using minimum delay Vedic real multiplier architecture," 2016 IEEE Uttar Pradesh Section International Conference on Electrical, Computer and Electronics Engineering (UPCON), Varanasi, 2016, pp. 580-584.

[8] Li-Rong Wang, Shyh-Jye Jou and Chung-Len Lee, "A well-structured modified Booth multiplier design," 2008 IEEE International Symposium on VLSI Design, Automation and Test (VLSI-DAT), Hsinchu, 2008, pp. 85-88.

[9] S. Patil, D. V. Manjunatha and D. Kiran, "Design of speed and power efficient multipliers using vedic mathematics with VLSI implementation," 2014 International Conference on Advances in Electronics Computers and Communications, Bangalore, 2014, pp. 1-6.