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Design and Verification of I2C Protocol using DUC and DDC

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Abstract: ***I2C or Inter-Integrated Circuit is a synchronous, serial communication protocol. I2C protocol is a Bi-directional communication protocol. I2C is a Multi-Master, Multi-Slave communication protocol designed by NXP semiconductors. This paper provides the literature Survey of I2C and Digital Up/Down Converters and Proposed method for Designing of I2C communication protocol and verification by using DUC (Digital Up Converter) and DDC (Digital Down Converter). I2C communication can be verified by using DUC and DDC. DDC which is the Receiver is designed based on WIMAX approach. DUC, which is the Transmitter, is done in MATLAB and again I2C is done in MATLAB. The transmission from DUC to DDC can be seen by using I2C communication Protocol. So, this paper provides the Literature Survey and Proposed method for the transmission from DUC to DDC using I2C protocol.***

Keywords: I2C; Verilog; SDA; SCL; FPGA; Digital Up Converter; Digital Down Converter; WIMAX; MATLAB; Transmitter; Receiver

I. INTRODUCTION

I2C is a two-wire, Synchronous Serial Communication protocol designed by Philips Semiconductor now termed as NXP Semiconductor.I2C is a Multi-Master, Multi-Slave communication protocol which can have as many masters and as many slaves in a system. It provides a Simple way to communicate between ICs in a shorter distance by using minimum number of pins. I2C bus uses two bidirectional signals, one as the Serial clock (SCL) line and other as the serial data (SDA) line.

The I2C standard includes collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus at the same time. Applications of I2C include Microcontrollers, PDA (Personal Digital Assistants), LCD, memory devices, PCs, cellphones, Television, ADCs (Analog to Digital Converters), DACs (Digital to Analog Converters), other slower and faster devices.

There exists many other Serial communication like SPI (Serial Peripheral Interface), UART (Universal Asynchronous Receiver Transmitter), Recommended Standards such as RS-232, RS-422, RS-485 and SPI (Serial peripheral interface), Microwire for interfacing high speed and low speed peripherals. These protocols require more pin connection in the IC (Integrated Circuit) for serial data communication to take place, as the physical size of IC have decreased over the years, we require less amount of pin connection for serial data transfer. In order to overcome this problem, the I2C protocol was introduced by Phillips Semiconductors or NXP semiconductors which requires only two lines for communication which makes the circuit simple and can control a network of device chips with just a two general purpose I/O pins whereas, other bus protocols require more pins and signals to connect devices.

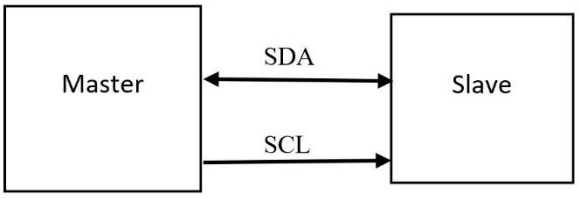

Fig 1. I2C Communication between Master and Slave

II. LITERATURE SURVEY

A. *Paper Title: Implementation Of I²C Multi Task And Multi Slave Bus Controller Using Verilog*

Authors: Shaik. Fazil Ahmed Y Murali

This paper shows the communication between FPGA (Field Programmable Gate Array) as a Master and MAXIM DS1307, which act as a Slave using I2C Master bus controller. The module here was Designed in Verilog HDL, simulated in ModelSim 10.1c and was Synthesized in Xilinx ISE Design Suite 14.2. This paper implements a Serial data communication between FPGA and MAXIM DS1307, which supports a bi-directional, 2-wire bus and data transmission protocol. This paper shows that any low speed peripheral devices can be interfaced using I2C bus protocol as master. It shows communication between single master, single slave which makes it a drawback, since I2C is a multi-master multi-slave protocol, another slave could have been used here.

B. *Paper title: Design and Modeling of I²C Bus Controller Using VHDL.*

Authors: Pankaj Kumar Mehto, Ashish Radhuvansi, Sonu Lal

This paper shows the communication between Microcontroller (Master) and EEPROM (Slave) using I²C protocol. The complete module of I²C bus controller is

designed in VHDL and simulated in ModelSim. The design is also synthesized in Xilinx XST 14.1. The design of I2C controller using VHDL, simplifies the design process. The Author also tells here that if a new technology emerges, then designer do not require to redesign the circuit. He can plainly input the intend program to the logic synthesis tool and it creates a new gate level netlist using the new fabrication equipment. The judgment synthesis tool will optimize the circuit in area and timing for the new technology. But he has not told about the new technology in the paper, which makes it a drawback.

C. *Paper title: High Speed & High Frequency based Digital Up/Down Converter for WCDMA System*

Authors: Arun Raj S.R

This paper shows FPGA implementation of Digital Down converters and Digital up converters for a single carrier WCDMA System. The DDC and DUC circuits were designed and implemented on spartan-3. The FPGA used is Spartan-3. Here the transmission is shown from DDC to DUC. WCDMA signal at IF 23.04 MHz is generated using the signal generator and applied to the ADC. Then ADC is connected to DDC then to DUC and finally to DUC for WCDMA signal.

D. *Paper Title: SPI to I2C Protocol Conversion using Verilog*

Authors: Dvijen Trivedi, Aniruddha Khade, Kashish Jain, Ruchira Jadhav

This paper shows a Design of Protocol Conversion Unit (PCU), which consists of a Serial In Parallel Out (SIPO) register and an I2C master device. It shows the communication between two widely accepted serial communication protocols SPI and I2C. Here, the sender is working on SPI and Receiver is working on I2C. so PCU communicates between these two protocols which has different number of pins and different communication schemes also. But here the Author tells that this can be upgraded using FIFO queue in PCU. But he doesn't tell about the application of PCU, which makes it a drawback.

E. *Paper Title: Digital Up and Down Converter for High Performance VHF and UHF Transceiver.*

Authors: Pavel Kovar, Pavel Puricer, Tomas Morong, Filip Šturc

This paper shows the DDC/DUC for dual mode professional VHF (very high frequency) and UHF (ultra-high frequency) Transceiver. Here the DUC is implemented by using the interpolation filter, NCO and mixers and DUC is also implemented by using the Decimation filter, NCO and mixers. Here, the proposed DUC/DDC is designed for standard intermediate frequency 45 MHz. which enables to use relatively cheap but high performance 16 bits ADC for direct sampling of the intermediate signals.

F. *Paper Title: Design of Arbitrated I2C Protocol with DO-254 Compliance.*

Authors: Bharath.K.B, K. V. Kumaraswamy, Roopa K Swamy

This Paper shows the design of Arbitrated I2C Protocol with DO-254 compliance. I2C is a multi-master communication protocol, it requires Arbitration technique. Since, only one master can be present in the communication with the slave. Such a technique is called Arbitration. The Author tells that DO-254 standard provides an assurance for the design with reliability, reusability and assurance for the design which can be used for real time applications like airborne, military, and avionics application. So this paper implements Arbitrated I2C protocol with DO-254 compliance.

G. *Paper title: Efficient ASIC Design of Digital Down Converter for Mobile Applications*

Authors: Rajesh Mehra, Shallu Sharma, Akanksha Jetly, Rita Rana

This paper shows the ASIC design of Digital Down converter using 90nm technology for software defined applications. The proposed method here for Digital Down Converter ASIC has consumed 601 mm2 area by consuming 3169.607nW power to provide high performance optimized solution to software defined radios. Usually, the Multiplier based partially serial algorithm for DDC is used to enhance the performance in terms of area and power consumption. Multipliers and adders are optimally placed and routed here in order to reduce the silicon area. The ASIC realization of the proposed design done here in this paper to find the power consumption of the DDC circuit. The Author tells that it achieves minimum power consumption. The ASIC DDC design was effectively Floor-planned and Routed to achieve the desired timing constraints.

H. *Paper title: Design of Dual Master I2C Bus Controller and Interfacing it with DC Motor.*

Authors: Deepika, Neetika Yadav

This paper shows the communication between FPGA and DC motor by using Dual master Bus controller. In order to implement this, first normal single master single slave is designed then by using Arbitration technique Dual master Bus controller is designed. Thus, the Author tells that the dual master I2C bus technique was implemented by using Arbitration technique. The design was first simulated using ModelSim and then synthesized using Xilinx ISE design suite. Finally, the synthesized design, obtained on FPGA, is interfaced with DC motor, which acts as a slave device for the masters. The direction of rotation of the DC motor has been controlled by the two masters.

I. *Paper Title: An Implementation of a WiMAX Based Digital Down Converter*

Authors: Vinay R. Gowda, Dr. C. R. Byrareddy

This Paper shows the implementation of DDC using WIMAX (Worldwide Interoperability for Microwave Access) approach. DDC usually consists of decimation FIR filters, NCO and Mixers. Here, the NCO (numerically controlled oscillator) is implemented using CORDIC approach. FIR filter used here is folded FIR Filter. The designed simulated in ModelSim using Verilog and transmitter part (DUC) is done in MATLAB. And also the paper shows the comparison between DDC based on Unfolded FIR filters, LUT based NCO and CORDIC based NCO, folded FIR filter. Thus, the Author tells that the Method based on CORDIC and folded FIR Filter yields low area and low power consumption. But here the communication (Transmission) is missing between DUC and DDC which may be a drawback.

J. Paper title: I2C Protocol Design for Reusability

Author: Zheng-wei HU

This paper shows one design method for I2C Reusability. The method proposed has 3 levels: protocol level, signal level and interface level. The design method of I2C protocol for reusability was proposed and was designed in VHDL and applied in bio-logging design which are based on I2C protocol. This paper shows the emulation by FPGA with light sensor and RTC. The Author tells that the data acquired by light sensor was transferred through RS232 to PC and stored into text file. The file was shown into graph by using MATLAB. The data acquired by RTC were shown by RS232 tool. The simulation results indicated this method is correct and efficient. One of the drawbacks is that the application for which it is used is very much limited. And another drawback is since it uses 3 levels in the proposed method, area becomes a major issue and power consumed is also more.so it becomes a drawback.

III. PROPOSED METHOD

Digital up converters and Digital down converters are the very important building block in any RF communication system. I2C is a simple serial Synchronous data communication protocol.

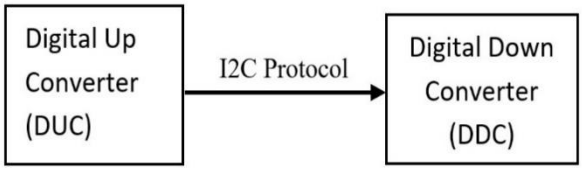

Fig 2. Communication between DUC and DDC

The two blocks which are important in front end signal processing unit in any RF communication system are DUC and DDC. The channel through which the intermediate frequency signal passes from DUC to DDC is I2C protocol as shown in Fig. 2. The transmission can be established between them as shown. I2C protocol can be designed using FSM (Finite state machine), based on this Verilog code can be written and Design and simulation can be done in Xilinx or in ModelSim.

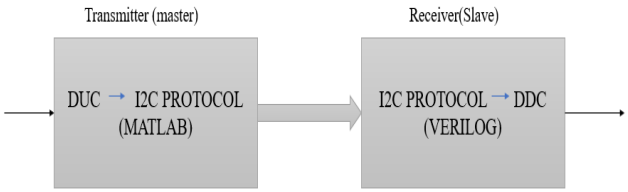

Fig 3. The Proposed method

Here the transmission between DUC and DDC can be obtained as shown in the Proposed method. In Proposed method, transmitter part is DUC which is the master and Receiver part is DDC which is the slave as shown in Fig. 3. DDC can be implemented based on WIMAX (Worldwide Interoperability for Microwave Access) approach, NCO is designed based on CORDIC method. Designing of DDC can be simulated using Verilog in ModelSim. DUC can be done in MATLAB. The transmission between DUC (Transmitter) and DDC (Receiver) by using I2C communication protocol can be seen as the result. Since DUC and DDC are used in almost all communication systems and I2C being a simple serial Data communication protocol, it has many applications in communication system. Thus, the verification of I2C protocol can be done in this method.

IV. CONCLUSION

The transmission from DUC to DDC using I2C can be made possible. Since, I2C is a simple serial data communication protocol has only two wires, so can be used in shorter distance communication. First, the I2C design can be done in Verilog using Xilinx or ModelSim. Then, DUC and DDC can be used for verification of I2C protocol. DUC and DDC are the main blocks in any communication systems. DDC block is based on WIMAX approach. NCO in DDC is based on CORDIC approach. FIR filter is a Folded FIR filter. So, thus DDC can be Designed using ModelSim. DUC block can be done in MATLAB. So, verification can be done by using DUC and DDC through I2C protocol.

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